OV7850/OV10626

datasheet

PRODUCT SPECIFICATION

1/3.2" color CMOS WVGA (744 x 520) high dynamic range (HDR) high definition (HD) image sensor

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color CMOS WVGA (744x520) high dynamic range (HDR) high definition (HD) image sensor

datasheet (mCSP)
PRODUCT SPECIFICATION

version 2.01
september 2017

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applications

- security and surveillance cameras
- 360 degree view applications
- rear view cameras
- night view cameras

ordering information

- **OV07850-N02A** (color, lead-free)
  102-pin mCSP™, rev 1E, packed in tray
- **OV07850-N02A-PE** (color, lead-free)
  102-pin mCSP™, rev 1E, packed in tray with protective film

features

- support for image size: WVGA, VGA, QVGA and any cropped size
- high dynamic range
- high sensitivity
- safety features
- low power consumption
- image sensor processor functions: automatic exposure/gain control, automatic white balance control, lens correction, defective pixel cancelation, HDR combination and tone mapping, automatic black level correction
- supported output formats: YUV, RAW, CCIR656
- horizontal and vertical sub-sampling
- serial camera control bus (SCCB) for register programming
- SPI master for overlay and loading settings
- external frame synchronization capability
- 50/60 Hz flicker cancellation
- parallel 16-bit DVP output
- NTSC with overlay and analog output

note To reduce image artifacts from infrared light, and provide the best image quality, OmniVision recommends an IR cut filter

key specifications (typical)

- **active array size:** 752 x 548
- **power supply:**
  analog: 3.14~3.47V
  core: 1.425~1.575V
  I/O: 1.7~3.47V
- **power requirements:**
  active: 410 mW typical @ 3.3V AVDD, 1.5V DVDD, and 1.8V DOVDD
  standby: 260 µW typical @ 3.3V AVDD, 1.5V DVDD, and 1.8V DOVDD
- **temperature range:** (see table 9-2)
  operating: -30°C to +85°C junction temperature
  stable image: 0°C to +50°C junction temperature
- **output interfaces:** 16-bit parallel DVP, analog NTSC (single end and differential)
- **input clock frequency:** 6 ~ 27 MHz
- **output formats:** up to 20-bit combined RAW, separated 8/10-bit RAW, 8-/10-bit YUV422
- **lens size:** 1/3.7" for VGA and NTSC, 1/3.2" for WVGA
- **lens chief ray angle:** 9° (see figure 11-2)
- **scan mode:** progressive
- **shutter:** rolling shutter
- **maximum image transfer rate:** 60 fps full resolution
- **sensitivity:** 16 V/Lux-sec
- **max S/N ratio:** 41 dB
- **dynamic range:** 120 dB
- **pixel size:** 6 µm x 6 µm
- **image area:** 4608 µm x 3384 µm
- **package dimensions:** 7310 µm x 7810 µm

note OmniVision recommends mCSP packages use underfill as part of camera assembly process.

note Since it is impossible to check compatibility with all displays, check the interoperability before committing to mass production.

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1 application system

1.1 overview

The OV7850 is a 1/3.2" optical format, 744x520 single-chip, low power CMOS, active-pixel, digital, high dynamic range sensors for both human vision and machine vision automotive applications.

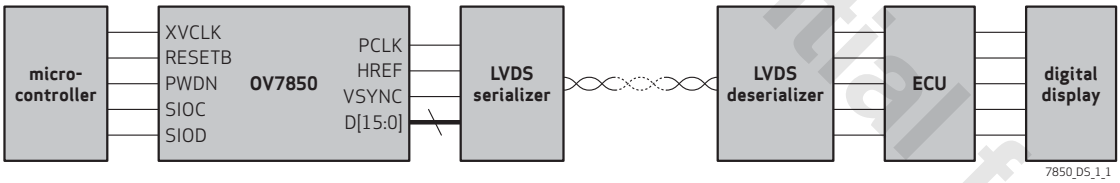
The OV7850 features OmniPixel3-HS™ technology to extend the dynamic range. The on-chip AEC/AGC automatically adjusts the ratio of the exposure and gain of the sub-pixels based on the dynamic range of the scene. The combined HDR RAW format is best suited for machine vision applications, while the fully processed YUV output provides the optimized HDR rendering for human vision applications.

The OV7850 is a complete camera-on-a-chip. It performs sophisticated camera functions on-chip controlled via the Serial Camera Control Bus (SCCB) interface. This includes lens shading correction, auto white balance, HDR combination, defect pixel correction, color interpolation and correction, de-noise and sharpening, gamma correction and tone mapping. It enables advanced HDR imaging in a simple, cost effective system.

1.1.1 typical OV7850 standalone camera

figure 1-1 is the block diagram of a standalone OV7850 camera for automotive applications. The micro-controller programs the register settings and controls the OV7850 based on the application requirements. The LVDS serializer and deserializer (SerDes) pair is for transferring video from the camera to the display unit over a long distance.

figure 1-1 standalone camera block diagram for automotive applications



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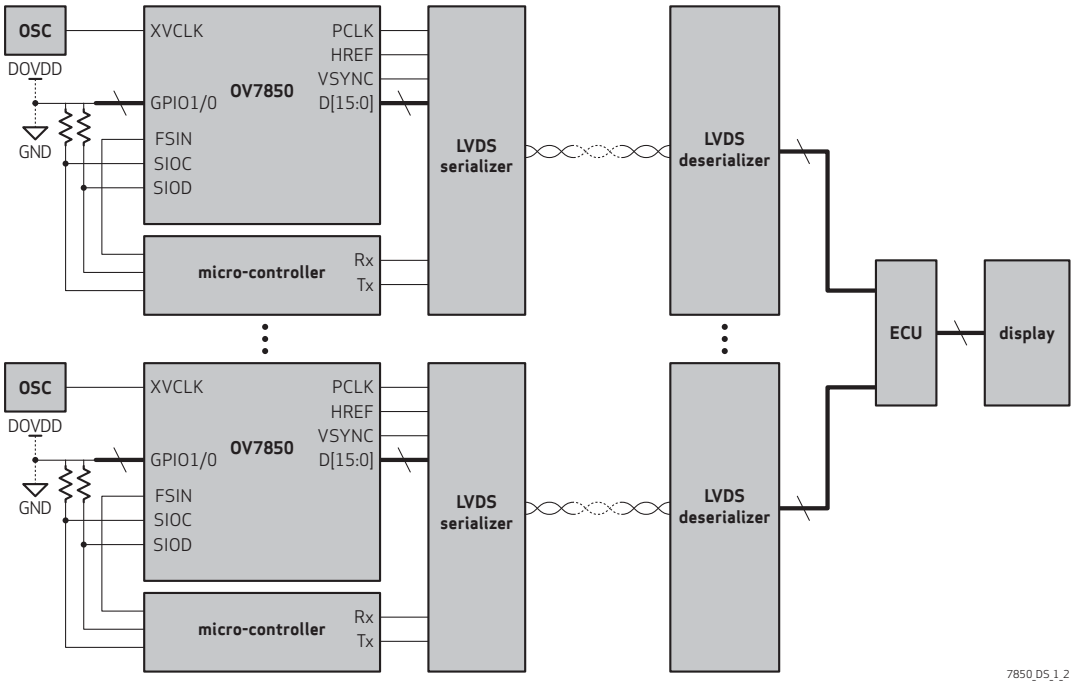
1.1.2 typical OV7850 multi-camera system

The OV7850 features frame sync input to synchronize the video streaming timing between multiple sensors in a multi-camera system. Up to four SCCB IDs can be selected by GPIO1/0 in case a unique SCCB ID is required to access each sensor. **figure 1-2** shows the block diagram of a typical multi-camera system using the OV7850. The sensor registers are programmed by the Electronic Control Unit (ECU) from the LVDS back channel. There can also be a local micro-controller in each camera and the ECU can control the sensor via the micro-controller.

figure 1-2 multi-camera block diagram



1.2 signal description and pin assignment

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7850 image sensor. The package information is shown in **section 10**.

table 1-1 signal descriptions (sheet 1 of 4)

pin number	signal name	pin type	description
A1	DOGND	ground	I/O ground
A3	DOGND	ground	I/O ground
A4	**GPIO0**	I/O	general purpose I/O
A5	DOVDD	power	I/O power
A6	**VMONL**	analog I/O	brown-out threshold voltage
A7	AVDD	power	analog power
A8	VH	analog I/O	analog reference
A9	AGND	ground	analog ground
A11	AGND	ground	analog ground
B2	DOGND	ground	I/O ground
B10	AGND	ground	analog ground
C1	DOGND	ground	I/O ground
C3	DOGND	ground	I/O ground
C4	**TMCLK**	input	input clock for test mode
C5	DOVDD	power	I/O power
C6	**VMON**	analog I/O	brown-out threshold voltage
C7	AVDD	power	analog power
C8	VH	analog I/O	analog reference
C9	AGND	ground	analog ground
C11	AGND	ground	analog ground
D1	DOVDD	power	I/O power
D3	DOVDD	power	I/O power
D4	**PWDNB**	input	power down (active low with pull up resistor)
D5	**TM**	input	test mode (active high with pull down resistor)
D6	**FLG**	output	brown-out threshold voltage

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table 1-1 signal descriptions (sheet 2 of 4)

pin number	signal name	pin type	description
D7	ATEST	analog I/O	analog test I/O
D8	NC	–	no connect
D9	AVDD	power	analog power
D11	AVDD	power	analog power
E1	**SIOC**	input	SCCB interface input clock
E3	**FSIN**	input	frame sync
E4	**RESETB**	input	reset/power down (active low with pull up resistor)
E5	**GPIO1**	I/O	general purpose I/O
E6	DVDD	power	digital circuit power
E7	**XVCLK**	input	system clock input
E8	SVDD	power	analog pixel array power
E9	**XI**	input	XTAL oscillator amplifier input
E11	**XO**	output	XTAL oscillator amplifier output
F1	**OVLEN**	input	SPI enable (OSD enable)
F3	**ESI**	input	SPI data input
F4	**SIOD**	I/O	SCCB interface data
F6	AGND	ground	analog ground
F7	EGND	ground	PLL ground
F8	EVDD	power	PLL digital power
F9	PVDD	power	PLL analog power
F11	PVDD	power	PLL analog power
G1	**CS**	output	SPI chip select
G3	DOVDD	power	I/O power
G4	DOGND	ground	I/O ground
G5	OGND	ground	NTSC DAC ground
G6	**D2**	I/O	video data output
G7	DOGND	ground	I/O ground
G8	DOVDD	power	I/O power
G9	DOGND	ground	I/O ground
G11	**PCLK**	I/O	video output clock

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table 1-1 signal descriptions (sheet 3 of 4)

pin number	signal name	pin type	description
H1	**ESO**	output	SPI data output
H3	DVDD	power	digital circuit power
H4	**SCK**	output	SPI clock
H5	DVDD	power	digital circuit power
H6	DOGND	ground	I/O ground
H7	**D14**	I/O	video data output
H8	**BPREG**	input	bypass internal 1.5V voltage regulator (active high)
H9	DVDD	power	digital circuit power
H11	**HREF**	I/O	video output horizontal sync signal
J1	DOVDD	power	I/O power
J3	DOVDD	power	I/O power
J4	OVDD	power	NTSC DAC power
J5	DOVDD	power	I/O power
J6	DVDD	power	digital circuit power
J7	**D7**	I/O	video data output
J8	**D15**	I/O	video data output
J9	DVDD	power	digital circuit power
J11	DVDD	power	digital circuit power
K1	**VRES**	analog I/O	NTSC DAC reference current program (high-z, if not used)
K3	**VCON**	analog I/O	negative NTSC analog video output (high-z, if not used)
K4	**VCOP**	analog I/O	positive NTSC analog video output or single ended NTSC analog video output (high-z, if not used)
K5	**D1**	I/O	video data output
K6	**D4**	I/O	video data output
K7	DVDD	power	digital circuit power
K8	DOVDD	power	I/O power
K9	**D12**	I/O	video data output
K11	**D13**	I/O	video data output
L1	DOGND	ground	I/O ground

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table 1-1 signal descriptions (sheet 4 of 4)

pin number	signal name	pin type	description
L3	DOGND	ground	I/O ground
L4	**VSYNC**	I/O	video output vertical sync signal
L5	DOVDD	power	I/O power
L6	**D5**	I/O	video data output
L7	**D9**	I/O	video data output
L8	**D11**	I/O	video data output
L9	DOGND	ground	I/O ground
L11	DOGND	ground	I/O ground
M2	DOGND	ground	I/O ground
M10	DOGND	ground	I/O ground
N1	DOGND	ground	I/O ground
N3	DOGND	ground	I/O ground
N4	**D0**	I/O	video data output
N5	**D3**	I/O	video data output
N6	**D6**	I/O	video data output
N7	**D8**	I/O	video data output
N8	**D10**	I/O	video data output
N9	DOGND	ground	I/O ground
N11	DOGND	ground	I/O ground

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table 1-2 pin states under various conditions (sheet 1 of 3)

pin number	signal name	RESETB=0	RESETB=1; PWDNB=1 stream/standby	RESETB=1; PWDN=0 power down (suspend)
A4	GPIO0	input	input (configurable)[a]	input (configurable)[a]
A6	VMONL	input	input	input
C4	TMCLK	input	input	input
C6	VMON	output	output	output
D4	PWDNB	input	input	input
D5	TM	input	input	input

table 1-2 pin states under various conditions (sheet 2 of 3)

pin number	signal name	RESETB=0	RESETB=1; PWDNB=1 stream/standby	RESETB=1; PWDN=0 power down (suspend)
D6	FLG	output	output	output
E1	SIOC	input	input	input
E3	FSIN	input	input	input
E4	RESETB	input	input	input
E5	GPIO1	input	input (configurable)[a]	input (configurable)[a]
E7	XVCLK	input	input	input
E9	XI	input	input	input
E11	XO	output	output	output
F1	OVLEN	input	input	input
F3	ESI	input	input	input
F4	SIOD	open-drain	open-drain	open-drain
G1	CS	output	output	output
G6	D2	output	output (configurable)[b]	output (configurable)[b]
G11	PCLK	output	output (configurable)[c]	output (configurable)[c]
H1	ESO	output	output	output
H4	SCK	output	output	output
H7	D14	output	output (configurable)[b]	output (configurable)[b]
H8	BPREG	input	input	input
H11	HREF	output	output (configurable)[c]	output (configurable)[c]
J7	D7	output	output (configurable)[b]	output (configurable)[b]
J8	D15	output	output (configurable)[b]	output (configurable)[b]
K1	VRES	output (high-z if not used)	output	output (high-z if not used)
K3	VCON	output (high-z if not used)	output (current)	output (high-z if not used)
K4	VCOP	output (high-z if not used)	output (current)	output (high-z if not used)
K5	D1	output	output (configurable)[b]	output (configurable)[b]
K6	D4	output	output (configurable)[b]	output (configurable)[b]
K9	D12	output	output (configurable)[b]	output (configurable)[b]
K11	D13	output	output (configurable)[b]	output (configurable)[b]

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table 1-2 pin states under various conditions (sheet 3 of 3)

pin number	signal name	RESETB=0	RESETB=1; PWDNB=1 stream/standby	RESETB=1; PWDN=0 power down (suspend)
L4	VSYNC	output	output (configurable)[c]	output (configurable)[c]
L6	D5	output	output (configurable)[b]	output (configurable)[b]
L7	D9	output	output (configurable)[b]	output (configurable)[b]
L8	D11	output	output (configurable)[b]	output (configurable)[b]
N4	D0	output	output (configurable)[b]	output (configurable)[b]
N5	D3	output	output (configurable)[b]	output (configurable)[b]
N6	D6	output	output (configurable)[b]	output (configurable)[b]
N7	D8	output	output (configurable)[b]	output (configurable)[b]
N8	D10	output	output (configurable)[b]	output (configurable)[b]

a. controlled through 0x302F after RESET high

b. automatically controlled according to driven value (0x3008, 0x3009) and output

c. manually controlled according to driven value (0x300D[7:5]) and output driver enable (0x3002[7:5]), by writing output driver select (0x3010[7:5]) when entering power down mode and resetting when entering streaming/standby

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figure 1-3 pin diagram

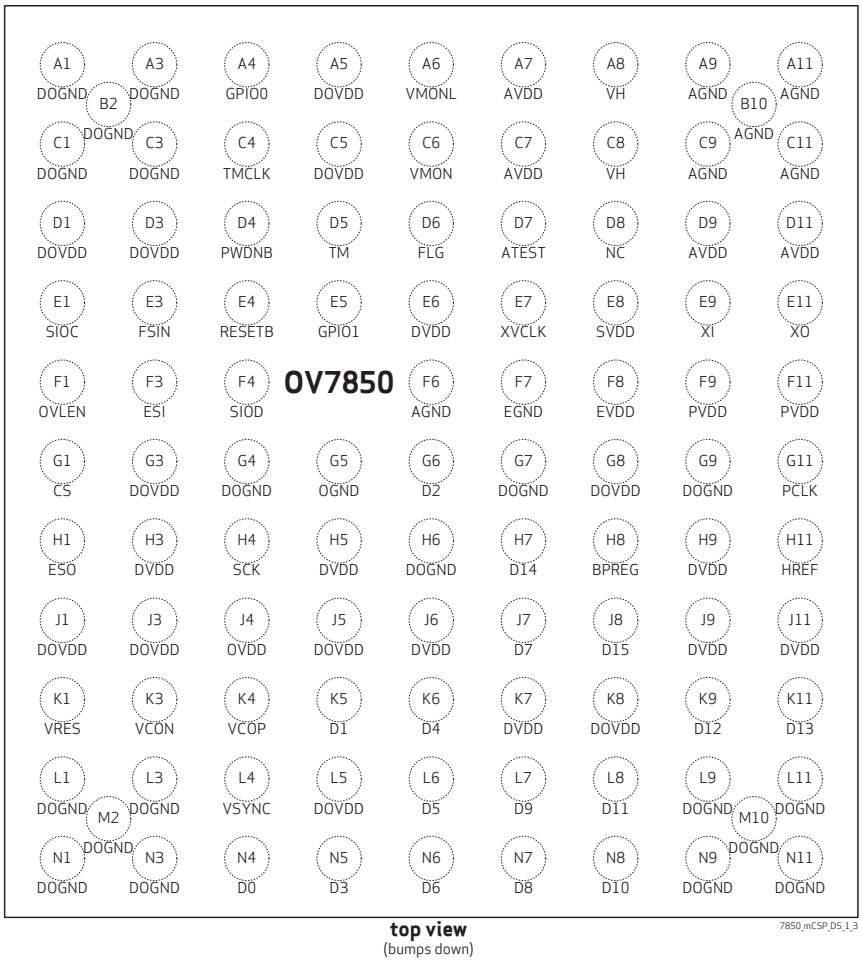


table 1-3 pad equivalent circuit (sheet 1 of 2)

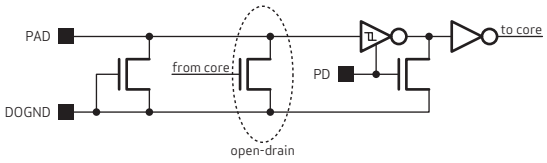
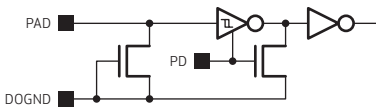
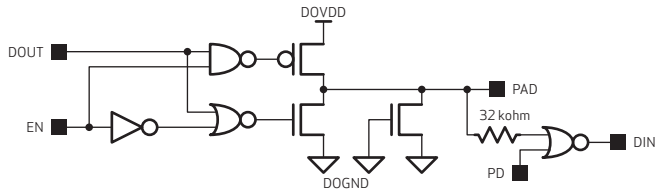
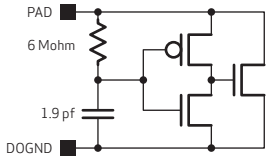
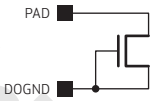
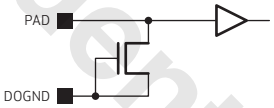
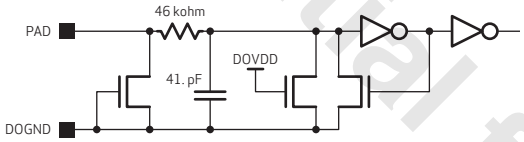
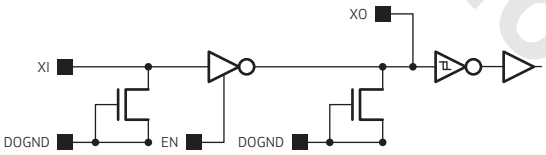
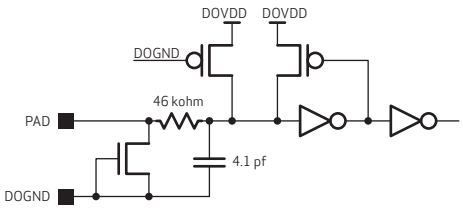
signal name	equivalent circuit
SIOD	
SIOC	

table 1-3 pad equivalent circuit (sheet 2 of 2)

signal name	equivalent circuit
D[15:0], PCLK, HREF, VSYNC, FSIN, GPIO, FLG, GPIO1, ESI, CS, ESO, SCK	
SVDD, AVDD, DOVDD, PVDD, DVDD, EVDD, OVDD	
DOGND, EGND, AGND, VH, OGND, VMONL, VMON, ATEST, VRES, VCON, VCOP	
XVCLK, TMCLK	
TM, OVLEN, BPREG	
XI, XO	
RESETB, PWDNB	

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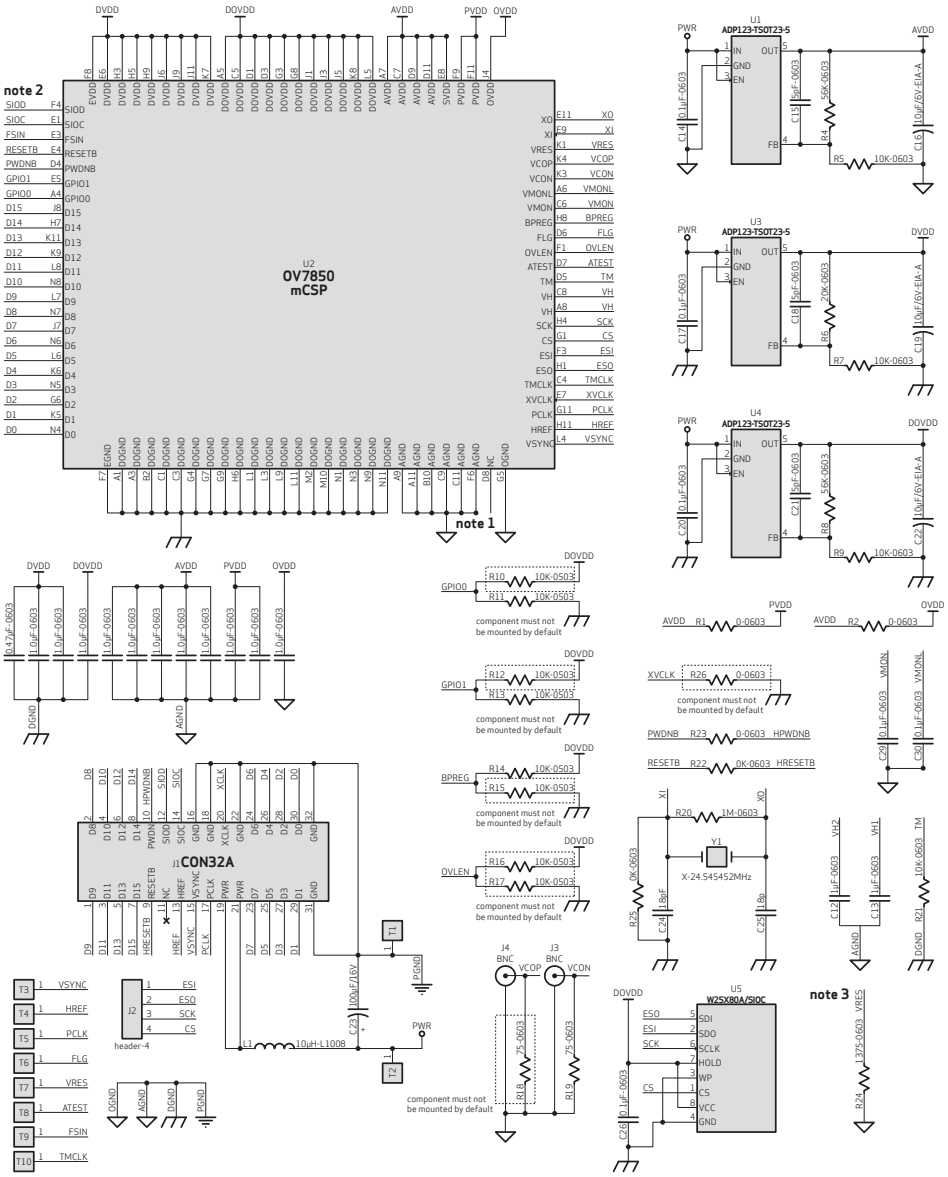
1.3 reference design

figure 1-4 shows the power supply and signal connection of the OV7850.

figure 1-4 OV7850 reference schematic



note 1 it is okay to connect D8 with AGND

note 2 if analog output interface is used and SCCB interface is not used, SIOC (SCCB clock) and SIOD (SCCB data) pins must be pulled up (either separately or tied together) and pulled up (10KOhm) to DOVDD

note 3 ± 1%

1.3.1 external components

The image sensor power is provided by 3.3V from system. The I/O pad power is 1.7~3.47V from system. The analog NTSC output power (OVDD) is 3.3V from system. An external resistor is used to program the NTSC voltage swing (output current). The core logic operates on 1.5V. The embedded linear voltage regulator can be used to generate 1.5V for the core logic when 1.8V is supplied for the I/O PAD power. For I/O pad power supply higher than 1.8V, an external regulator should be used to supply the 1.5V for the core logic. This limitation on using the embedded regulator is to avoid excessive heating from the power dissipated in the linear regulator. Refer to **table 9-3** for the voltage range and current consumption for each supply. When the internal crystal oscillator amplifier is used, the external crystal (and passive components) must be connected between the XI and XO pads, and the XVCLK must be connected to ground. When the sensor is not configured to use the crystal oscillator amplifier (i.e., external clock applied on the XVCLK pad), it is important to connect the XI pin to ground on the PCB. The OV7850 need external power de-coupling capacitors to reduce noise. The default capacitor value is 0.1μF, but for DVDD, a capacitor of 0.47μF (ESR<1Ω) is required when the embedded voltage regulator is used.

1.3.2 power on reset generation

The reset can be controlled from the external pin. However, inside this chip, there is a power on reset generation function to auto detect core power at stable state. There is also a brown-out detector on the AVDD power supply, the output from this circuit applied on an output pin, but is not connected internally in the chip.

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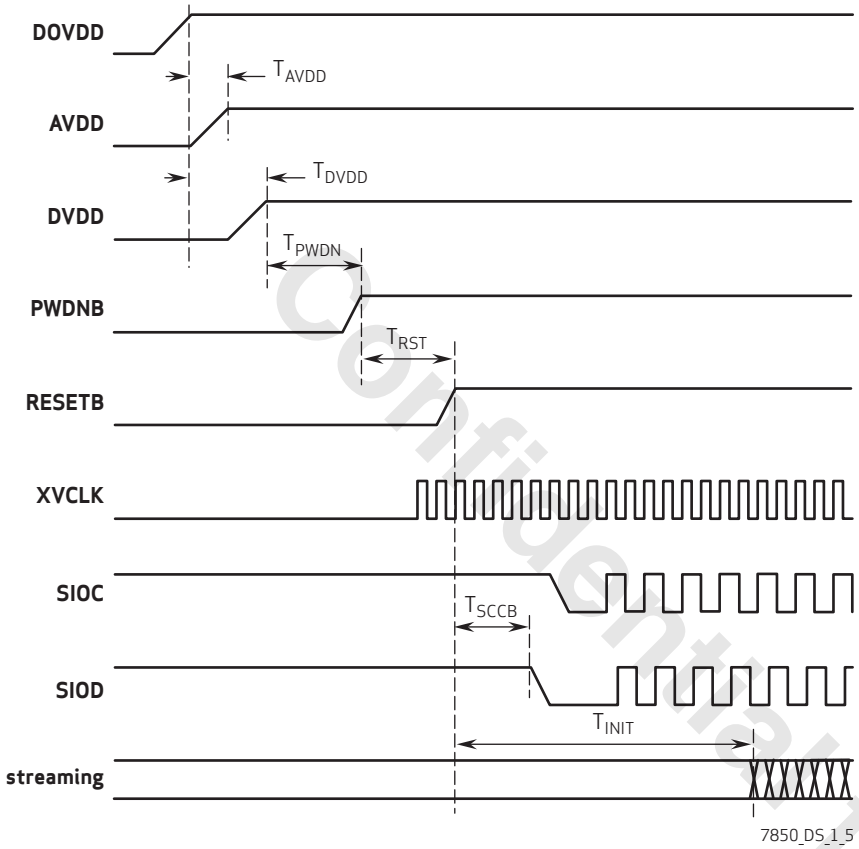
1.4 power up sequence/ boot sequence

figure 1-5 power on timing diagram



When power is applied to the chip, the analog POR module will keep the chip in reset mode until the voltage is high enough to start operation. When the analog POR is released an additional 255 XVCLK cycles are waited to give some extra time for the system to stabilize. To extend this period keep the RESETB pin low.

T_{SCCB} starts from RESETB going high or XVCLK present, whichever is last. The XVCLK must be stable before reset mode is released since reset mode release is clocked by XVCLK. The initialization delay (T_{INIT}) is a combination of the PLL lock time (~4096 XVCLK cycles) and initialization of internal register settings.

PVDD and OVDD should follow AVDD when power-up.

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table 1-4 power on timing

parameter	min	max	unit
T_{AVDD}	0	n/a	ms
T_{DVDD}	0	10	ms
T_{PWDN}	1	n/a	ms
T_{RST}	0	n/a	ms
T_{SCCB}	255	n/a	XVCLK cycles
T_{INIT}	26,000[a]	n/a	XVCLK cycles

a. This number is for normal case. If the OTP and/or SPI are used to load settings from a setting file, please send the setting file after the OTP and/or SPI loading has finished.

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1.4.1 power down sequence

When in standby mode, power down mode can be entered by pulling the PWDNB pin low. In this state, all internal clocks are gated and the internal regulator is set in a power-saving low-power mode. When the regulator resumes from low power mode 255 XVCLK cycles are waited before turning on any clocks to ensure safe operation. The power down mode can only be entered from the standby mode. If register 0x3105[2] or register 0x3105[3] (see **section 1.4.5**) is set, it is not possible to enter power down mode. DVDD should be turned off before DOVDD because current can be conducted from DVDD to DOVDD through the regulator when DOVDD is not supplied.

1.4.2 operating modes

The OV7850 supports following modes:

- reset mode
  - enabled when RESETB pin low
  - all modules brought to reset, including registers
  - IOs tri-stated
  - no active clocks
  - disabled SCCB
- power down mode (suspend mode)
  - enabled when PWDNB pin low
  - similar to reset mode, except register values are maintained
  - IOs de-activated (can be tri-stated or driven high or low by register control)
  - the clock input is blocked to internal circuit logic control
  - internal clocks stopped
  - all sensor modules powered off, including SCCB

- standby mode
  - asserted after power-up and after SCCB command register 0x303E[0]=0
  - all modules powered ON
  - pads are active
  - PLL stopped (if early activation is not enabled)
- streaming mode
  - image capture and output streaming enabled

1.4.3 activation sequence

After power-up, the chip enters standby mode. By setting register 0x303E[0]=1, the necessary analog modules and the PLLs are turned on. When the PLLs are stable after 4096 XVCLK cycles, the main clocks are switched from XVCLK to the faster PLL clock. When T_{init} is done, streaming is activated.

1.4.4 deactivation sequence

By clearing register 0x303E[0] when in streaming mode, the chip will enter standby after finishing the current frame (finish is signaled by VSYNC at the DVP-fifo). The main clock is switched from PLL to XVCLK clock. If early activation is not set, PLLs and analog modules are turned off.

1.4.5 early activation

For faster activation, the user can choose to power up the analog modules and PLLs in standby mode. To turn on the analog modules, set register 0x3105[2]. Since the PLLs are dependent on the analog to be powered up, register 0x3105[2] needs to be set for early PLL startup to work. Early PLL startup is enabled by setting register 0x3105[3].

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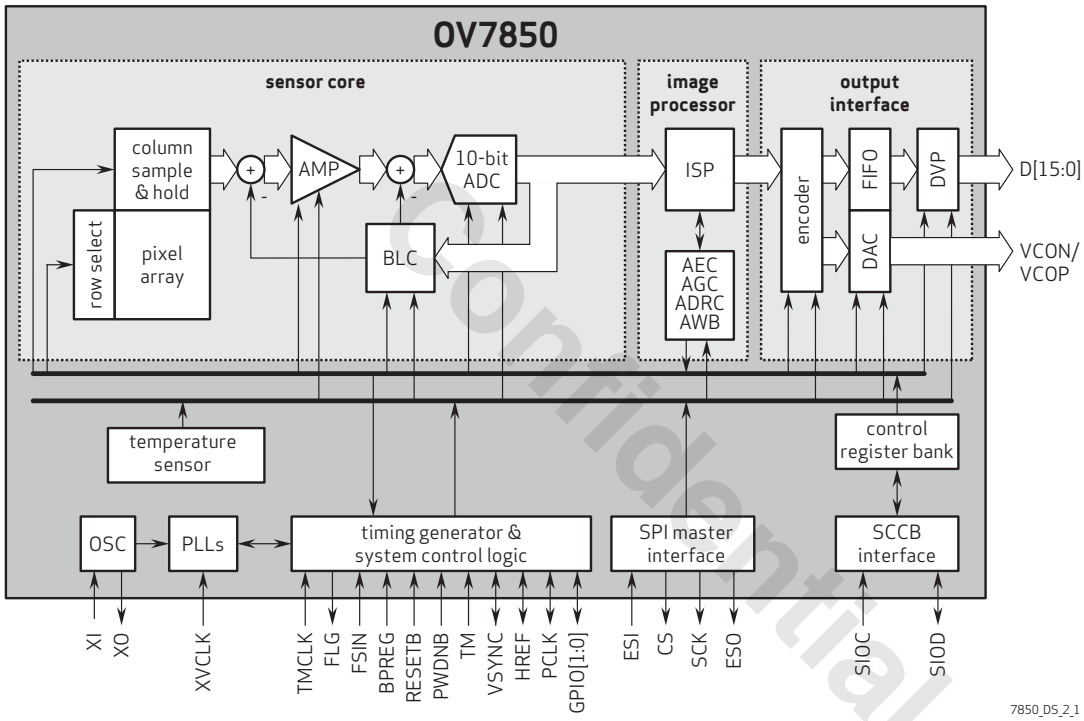
2 sensor architecture

figure 2-1 shows the top level block diagram of the OV7850 sensor.

figure 2-1 OV7850 block diagram



The sensor consists of three major functional blocks: the sensor core, the image processor, and the output interface.

The sensor core receives the photo signal which generates electrical charge collected by the pixel photo diodes (PDs). During readout, the accumulated charge is converted to a voltage signal in the pixel. This signal is then amplified and converted to a digital signal by the analog-to-digital converter (ADC). Dark current and circuit offsets are compensated by the black level correction circuit (BLC). The initial correction is implemented in analog domain in two steps, before and after amplification, to ensure optimal utilization of the dynamic range of the amplifier and the ADC. The final accurate correction is implemented purely in the digital domain. Dark current increases exponentially with temperature and the BLC can be configured to automatically re-trigger with changes in junction temperature, in addition to changes in gain. The sensor core supports readout of three exposure values; long (L), short (S), and very short (VS), that can be used to process a high dynamic range image (HDR). Each pixel constitutes of a large and small PD. The large PD (LPD) is used for the long and very short exposure channels, whereas the small PD (SPD) is used for the short exposure channel. The BLC runs separately on the three exposure channels.

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The video stream from the sensor core is applied to the image processor, which processes the data to generate the desired output format for the target display. Statistic data is calculated by the image processor and then applied to the automatic exposure control (AEC), automatic gain control (AGC), and automatic dynamic range control (ADRC) in order to control the exposure time and gain of the long, short, and very short exposure channels. The output from the three exposure channels are combined to create a HDR output image. The image processor also supports lens correction (LENC), defect pixel correction (DPC), de-noise (DNS), color interpolation (CIP), automatic white balance (AWB), and HDR tone mapping.

The processed image is formatted and output through the digital video port (DVP) interface or through the analog NTSC output. The supported output formats includes 8/10-bit processed YUV422, combined 16/18/20-bits HDR, and 8/10-bits RAW data for each of the three exposure channels. The analog output is driven by an on-chip digital-to-analog convertor (DAC) and the output current is converted to voltage by external termination resistors. An external resistor is also used to program the range of the DAC.

Two on-chip phase lock loops (PLLs) generate the required clock signals for all blocks from the XVCLK input clock or the output of the on-chip XTAL oscillator amplifier. The timing generator generates the control signals for the pixel array to reset the PDs at the beginning of the exposure, to stop the exposure by reading out the accumulated charge, and also to generate the required control timing for the readout amplifier and ADC. The horizontal synchronization reference (HREF), the vertical synchronization (VSYNC), and the pixel clock (PCLK) signals are also generated so the backend processor can receive the image data.

The serial peripheral interface (SPI) can be used to load the on screen display data (OSD) from an external memory. The SPI can also be used to load register settings. This can be utilized to program settings and start streaming in systems without host processor.

All functional blocks are controlled by registers. The host controller can program and read back through Serial Camera Control Bus (SCCB) interface.

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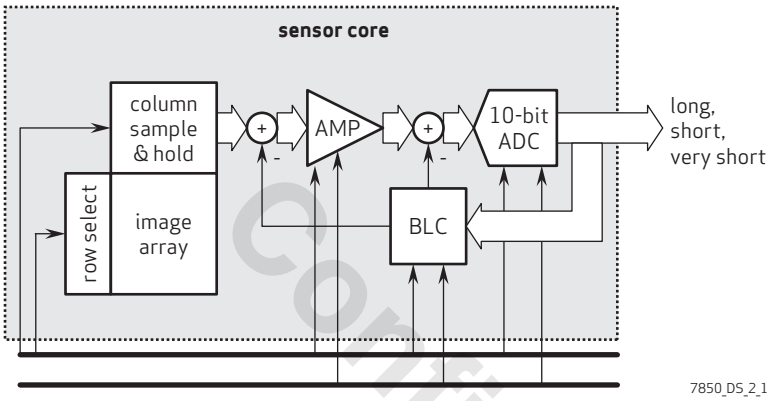
3 image sensor core

figure 3-1 shows the top level block diagram of OV7850 sensor core.

figure 3-1 sensor core block diagram



The analog sensor core consists of the active pixel array, the row access control circuit, the column sampling circuit, and the analog readout channel. The programmable gain voltage amplifier is used to amplify the output signal from the pixel array before it is applied to the analog-to-digital converter (ADC). The analog readout channel also supports subtraction of programmable offset voltage at the input of the voltage amplifier and at the input of the ADC. The offset subtraction is controlled by the black level correction circuit (BLC) which will be described in more details in **section 3.7**. A single analog readout channel is used for processing of the three exposure channels (L, S, VS). This provides the optimal matching between the exposure channels, but the readout channel needs to operate three times faster compared to standard single exposure scheme.

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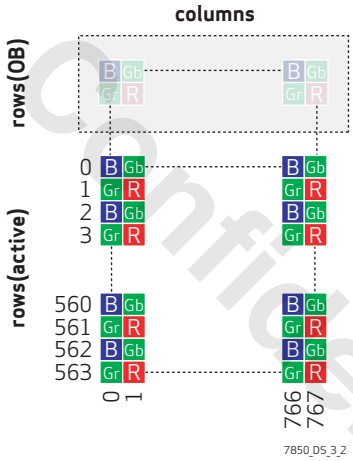
3.1 pixel array structure

The OV7850 sensor has an image array of 768 columns by 564 rows covered with color filters arranged in a Bayer pattern. **figure 3-2** shows the pixel array color filter layout. In addition to the active pixel rows, optical black (OB) pixel rows are embedded to serve as reference pixels for the black level correction (BLC). The OB rows are covered with a light shield (solid metal layer). In order to minimize non-ideal edge effects in the output image, it is not recommended to use the pixels at the lowest and highest row and column addresses.

figure 3-2 pixel array region color filter layout



Each pixel has two photo diodes (PDs) with independent exposure and gain controls to extend the dynamic range. The two PDs also have different size to provide different sensitivity. The large PD (LPD) provides high sensitivity and the small PD (SPD) provides low sensitivity. The OV7850 supports triple exposure readout, with two exposures in spatial domain, and the shortest exposure in time domain:

- long exposure (L) using the large photodiode (LPD), also used in linear (non-HDR) mode
- short exposure (S) using the small photodiode (SPD) with an exposure time of less than or equal to long exposure time
- very short (VS) using large photodiode (LPD), in the range of approximately 0.1 to 3.9 row time

The exposure time for S (T_S) will always start 4 rows or later after exposure time for L (T_L) start and finish 4 rows after T_L.

The exposure time for VS (T_{VS}) will always start after (T_L) finish. The sampling point is 4 rows after, but the T_{VS} start can move from end of T_L to just before sampling of T_{VS} (see **figure 3-3**).

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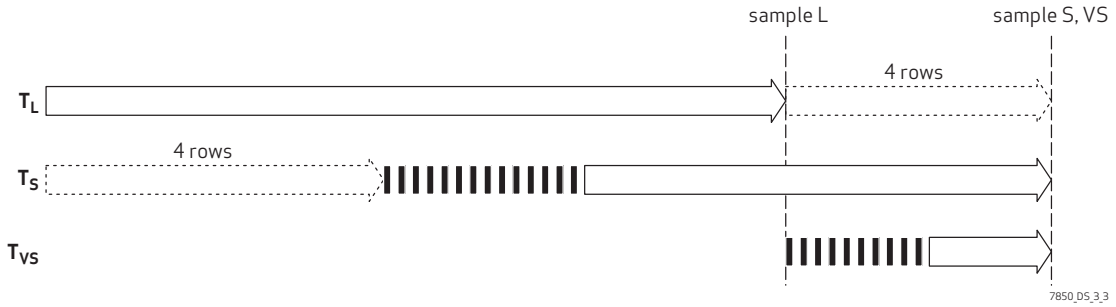
figure 3-3 exposure time diagram



The OV7850 can operate according to five sensor exposure modes:

- three exposure mode: HDR mode with all three exposures valid
- L,S exposure mode: HDR mode with only long and short exposures valid
- L,VS exposure mode: HDR mode with only long and very short exposure valid
- L exposure mode: linear mode using only L exposure
- traffic exposure mode: HDR mode, restrict short exposure to be sufficient long to capture LED traffic/car light

Refer to **section 5,** AEC/AGC algorithms for details.

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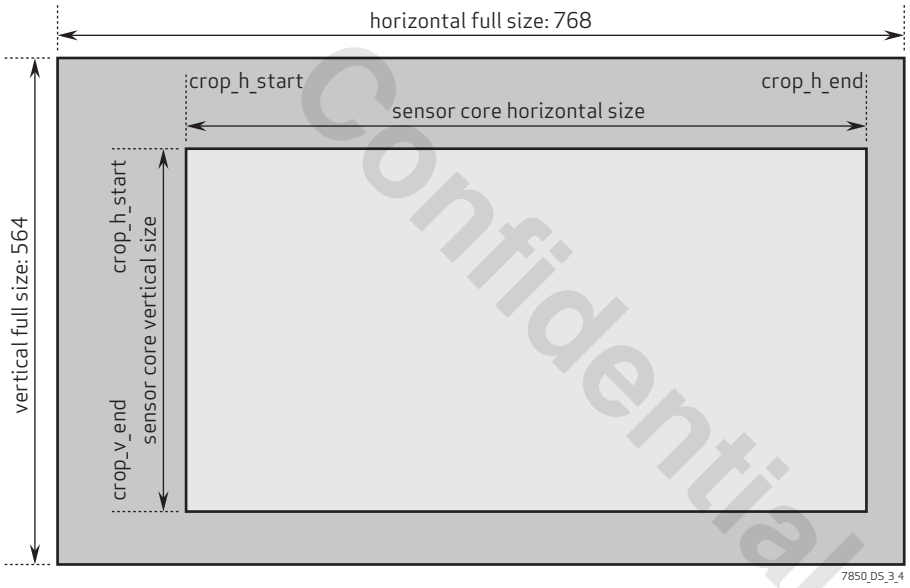
3.2 pixel array access

The readout window is fully programmable in horizontal and vertical direction, but should always start at an even row and column and stop at an odd row and column address in order to preserve the Bayer pattern order. The 'crop' address in registers 0x3800~0x3807 programs the sensor core readout window and can be set freely within the pixel array. The crop window is programmed larger than the processed output image resolution because the ISP uses extra rows and columns for the image processing algorithms (e.g., de-mosaic and defect pixel correction).

figure 3-4 pixel array access diagram



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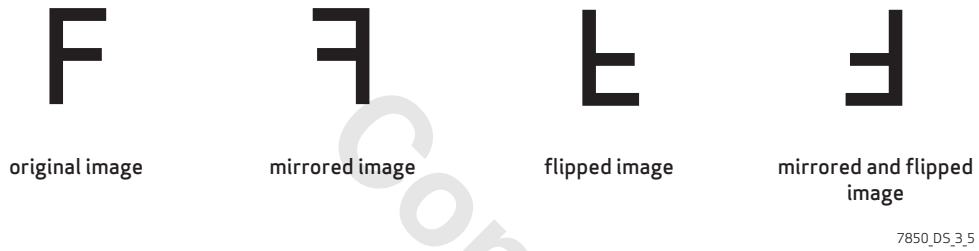
3.3 mirror and flip

The pixel array can be accessed in the reverse order in column and row direction (i.e., the image can be horizontally mirrored and vertically flipped) using registers 0x381C[3:2] and 0x5003[1:0]. Refer to **figure 3-5**.

figure 3-5 horizontal mirror and vertical flip samples



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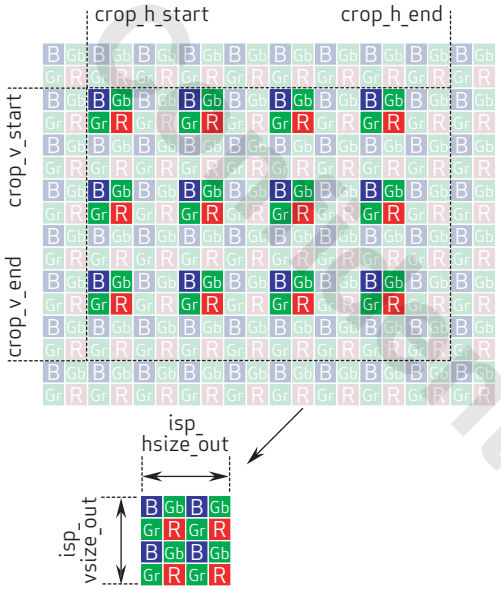
3.4 sub-sampling

The pixel array can be sub-sampled by a factor 2 in both horizontal and vertical directions, controlled by register 0x381C[1:0]. Sub-sampling is done in the sensor core. The ISP processes the output from the sensor core as a continuous stream of pixel values and generates a lower resolution output image. The horizontal and vertical sub-sampling can be programmed independently. The vertical sub-sampling enables a higher frame rate since the number of rows per frame is reduced, whereas the horizontal sub-sampling will not enable higher frame rate since the number of clock periods per row is not reduced when horizontal sub sampling is enabled.

figure 3-6 horizontal and vertical sub-sampling



note when using sub-sampling, the size (crop_h_end - crop_h_st+1) and (crop_v_end - crop_v_st + 1) must be multiple of four

7850_DS_3_6

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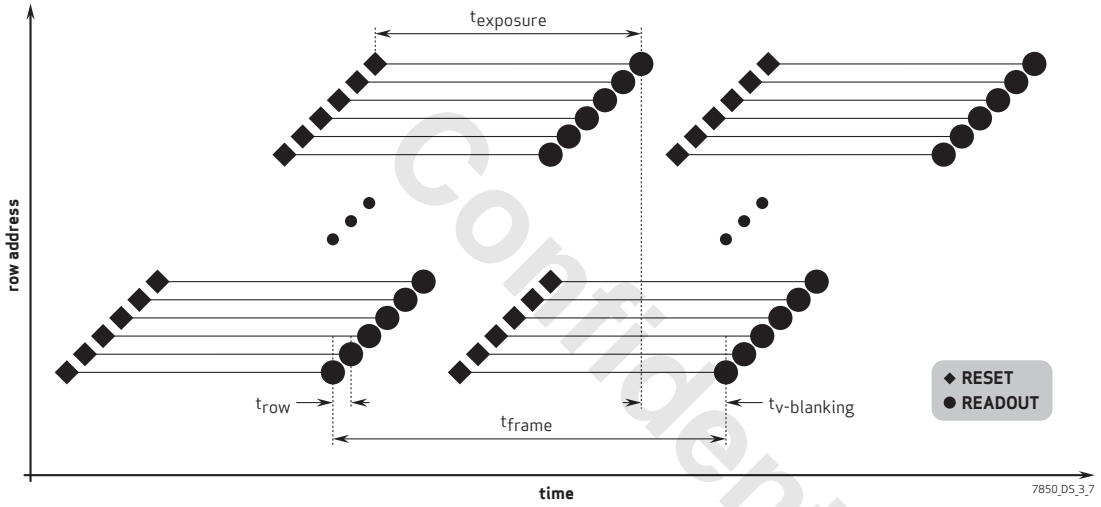
3.5 frame timing and maximum frame rate

The OV7850 employs an electronic rolling shutter for exposure control, refer to **figure 3-7**. The exposure time is determined by the AEC/AGC based on the luminance and dynamic range of the scene. The pixel array is first reset row by row and when the exposure time has elapsed, the readout of the pixel array is done row by row.

figure 3-7 row address versus time graph



The timing generator generates all the control signals based on a row counter and column counter. Refer to **figure 3-8** for the frame timing. The row period consists of an active output period and a horizontal blanking period. A vertical blanking period is also required to perform frame based operation. The vertical blanking period seen by the backend processor is usually longer than the internal vertical blanking because the BLC is reading the optical black rows required to perform the correction.

A minimum number of clock periods are required to complete all the required operations per row (blanking time). Refer to **section 6** for details.

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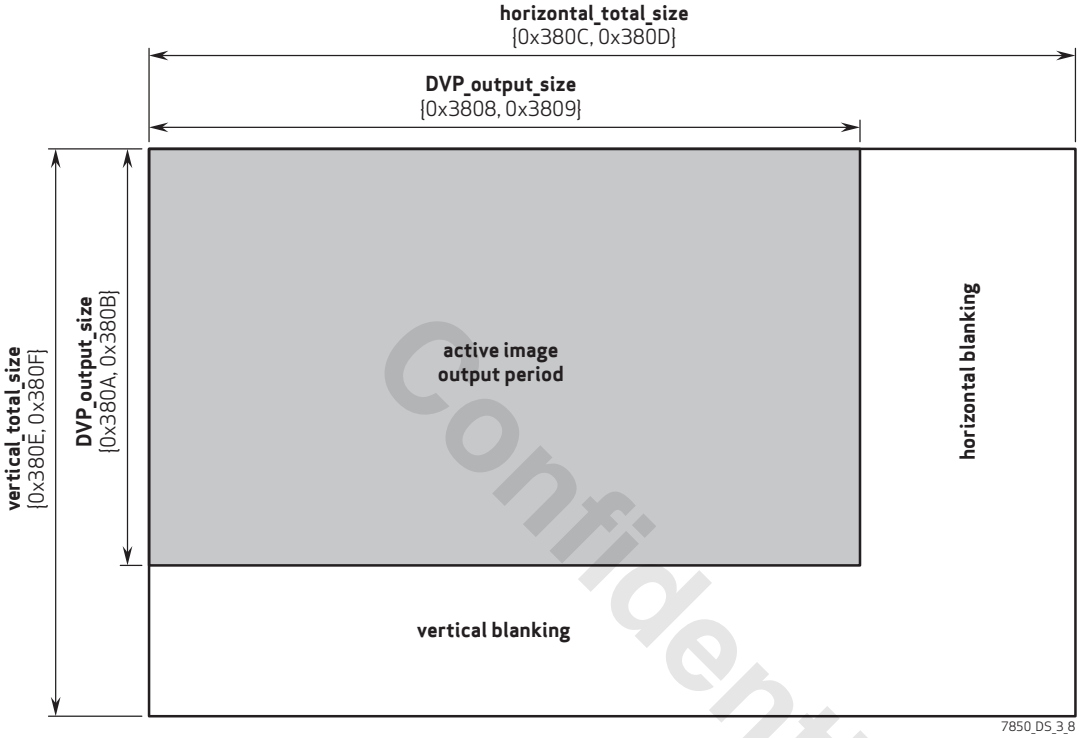
figure 3-8 frame output timing diagram



The maximum frame rate is determined by the maximum pixel clock, the total number of pixels read out of the entire frame and the minimum horizontal/vertical blanking time. The system clock and the minimum blanking time are usually fixed for a given design and the frame rate is dependent on the number of pixels read out. If the requested output image size (DVP output size) is smaller than the full pixel array, it is not necessary to read out the whole pixel array, thus, the frame rate can be increased by cropping and/or sub-sampling the pixel array (refer to **figure 3-3** and **figure 3-6**). **table 3-1** lists the most common image sizes and the maximum frame rates that the sensor can achieve. Other image sizes are also possible by cropping and/or sub-sampling. Refer to **section 6** output interface for details.

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table 3-1 DVP supported formats and frame rates[abcde]

format	pixel number	frame rate	methodology	pixel clock
full	744x520	60 fps	full progressive	54.9 MHz
full + border	760x528	60 fps	full progressive	55.7 MHZ
VGA	640x480	60 fps	DV format progressive	54.0 MHz
		60 fps	crop	48.0 MHz
QVGA	320x240	60 fps	crop and skip	48.0 MHz
		120 fps	crop and skip, but 32 lines not used for AEC, AGC, processing limitation	48.0 MHz
		120 fps	crop and skip, RAW mode	24.0 MHz
any size		60 fps	crop	54.0 MHz
NTSC		59.94 fps	analog NTSC	49.09 MHz[e]

a. pixel clock frequency is halved in RAW mode

b. OV7850 supports output format: 10-20-bit combined, 2x, 3x 10-bit RAW

c. all windowing must be in four pixels boundary

d. active array resolution (752x548) is larger than WVGA (744x520) to support mechanical alignment for VGA output format

e. 24.545452MHz input MCLK

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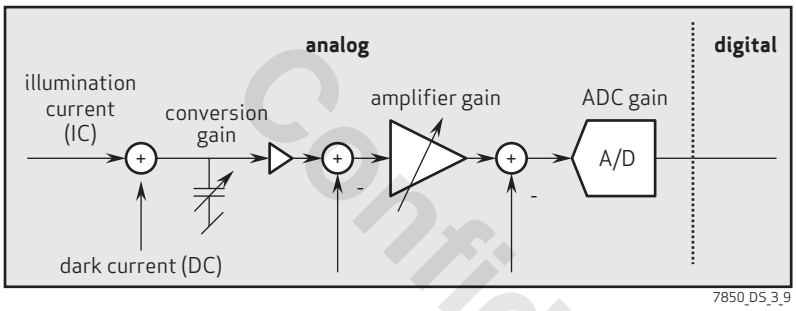
3.6 analog gain and ADC

The analog read out channel is identical for long (L), short (S), and very short (VS) exposure channels. The regular analog gain is programmable in the range 1-16x. The analog gain is a combination of amplifier gain (1, 2, 4, or 8x) and ADC gain which is achieved by programming the ADC reference voltage (1-2x, in steps of 1/32). In addition, LPD supports dual conversion gain with a conversion gain ratio is x3.14. **figure 3-3** shows the gain stages in the read out channel.

figure 3-9 gain stages diagram



The ADC resolution is 12-bits, but after BLC and digital correction, the resolution of the processed pixel values is reduced to 10-bits.

The applied gain can always be read from 0x3505-0x3507, see **appendix A** for details. For manual control see **section 5.5**.

table 3-2 timing control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	CROP_H_ST_H	0x00	RW	Bit[1:0]: Start address horizontal[9:8]
0x3801	CROP_H_ST_L	0x40	RW	Bit[7:0]: Start address horizontal[7:0]
0x3802	CROP_V_ST_H	0x00	RW	Bit[1:0]: Start address vertical[9:8]
0x3803	CROP_V_ST_L	0x22	RW	Bit[7:0]: Start address vertical[7:0]
0x3804	CROP_H_END_H	0x02	RW	Bit[1:0]: End address horizontal[9:8]
0x3805	CROP_H_END_L	0xCB	RW	Bit[7:0]: End address horizontal[7:0]
0x3806	CROP_V_END_H	0x02	RW	Bit[1:0]: End address vertical[9:8]
0x3807	CROP_V_END_L	0x11	RW	Bit[7:0]: End address vertical[7:0]
0x3808	DVP_H_SIZE_H	0x02	RW	Bit[7:0]: DVP horizontal size[15:8]

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table 3-2 timing control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3809	DVP_H_SIZE_L	0x88	RW	Bit[7:0]: DVP horizontal size[7:0]
0x380A	DVP_V_SIZE_H	0x01	RW	Bit[7:0]: DVP vertical size[15:8]
0x380B	DVP_V_SIZE_L	0xE8	RW	Bit[7:0]: DVP vertical size[7:0]
0x380C	HTS_H	0x03	RW	Bit[7:0]: Line length[15:8]
0x380D	HTS_L	0xE9	RW	Bit[7:0]: Line length[7:0]
0x380E	VTS_H	0x02	RW	Bit[7:0]: Frame length[15:8]
0x380F	VTS_L	0x0D	RW	Bit[7:0]: Frame length[7:0]
0x3810	WIN_HOFFS_H	0x00	RW	WIN_HOFFS_H
0x3811	WIN_HOFFS_L	0x08	RW	WIN_HOFFS_L
0x3812	WIN_VOFFS_H	0x00	RW	WIN_VOFFS_H
0x3813	WIN_VOFFS_L	0x04	RW	WIN_VOFFS_L
0x3814	RSVD	–	–	Reserved
0x3815	MIN_REQ_TIME_L	0x90	RW	Bit[7:0]: Minimum time use in sequencer[7:0]
0x3816	EXTRA_DELAY_H	0x00	RW	Bit[7:0]: Last row can be extended by this number
0x3817	EXTRA_DELAY_L	0x00	RW	Bit[7:0]: Last row can be extended by this number
0x3818	SENSOR_CTRL	0x00	RW	Bit[7:5]: Reserved Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3:0]: Reserved
0x3819~ 0x381A	RSVD	–	–	Reserved
0x381B	ABC_FLAG	0x00	RW	Bit[1:0]: abc_flag 00: A 01: B 10: C 11: Not used

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table 3-2 timing control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x381C	READ_MODE	0x00	RW	Bit[7:5]: hdr_mode 000: hdr_3exp 001: ls_2exp 010: lvs_2exp 011: l_1exp 100: traffic_3exp Bit[4]: Not used Bit[3]: Flip Bit[2]: Mirror Bit[1]: Vsub2 Bit[0]: Hsub2
0x381D	READ_CTRL	0x04	RW	Bit[2]: show_embedded_rows Bit[1]: show_test_rows Bit[0]: show_black_rows
0x381E~ 0x384F	RSVD	–	–	Reserved
0x3850	A_DAC	0x00	RW	Bit[5:0]: NTSC DAC control
0x3851	A_REGULATOR	0x00	RW	Bit[3:0]: Voltage regulator control
0x3852	A_TPM	0x00	RW	Bit[4]: Disable temperature monitor Bit[3:0]: a_tpm_ctrl
0x3853	A_BOD_H	0x02	RW	Bit[4:0]: brown_out control[12:8]
0x3854	A_BOD_L	0x10	RW	Bit[7:0]: brown_out control[7:0]
0x3880	EXPOSURE_LONG_H	–	R	Bit[7:0]: Frame long exposure (in rows)[15:8]
0x3881	EXPOSURE_LONG_L	–	R	Bit[7:0]: Frame long exposure (in rows)[7:0]
0x3882	EXPOSURE_SHORT_H	–	R	Bit[7:0]: Frame short exposure (in rows)[15:8]
0x3883	EXPOSURE_SHORT_L	–	R	Bit[7:0]: Frame short exposure (in rows)[7:0]
0x3884	EXPOSURE_VERY_ SHORT	–	R	Bit[6:0]: Frame very short exposure (in rows), form
0x3885	GROUP_HIT	–	R	Bit[3:0]: group_hit
0x3886	FCNT_H	–	R	FCNT_H
0x3887	FCNT_L	–	R	FCNT_L
0x3888~ 0x388C	RSVD	–	–	Reserved
0x388D	ABC_MODE_CURRENT	–	R	Bit[1:0]: Mode for current frame

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3.7 black level correction (BLC)

The black level correction (BLC) function is used to set the pixel output of a complete black object to a programmable pedestal value in all kinds of lighting conditions. Due to circuit offset and pixel dark current, the pixel output level of a black object is normally non-zero. The OV7850 calibrates the black level of the active pixel by subtracting the true optical black pixel output.

The target BLC pedestal value for the long, short and very short exposure channels are set by registers 0x3515 to 0x351A in 10-bit scale. The ISP will subtract the pedestal value early in the signal processing path. By default, the target pedestal values (0x3515 to 0x351A) are subtracted, but when the manual target is enabled (0x4002[6]=1), the ISP will subtract the manual pedestal value set by registers 0x400E to 0x4013 for the long, short, and very short exposure channels. The manual pedestal value can be relevant to use at high junction temperature to mitigate the artifact due to uneven dark current.

Enabling of the different BLC steps is controlled by registers 0x4000 and 0x4002. When BLC is enabled, the active pixel output value will be limited to 0x3FF after subtracting the optical black pixel value. When the BLC is disabled, no black pixel subtraction is performed.

Optical black rows are used for BLC and are not output in the final image, but enabling show_black_rows (0x381D[0]=1) will output the black rows in the beginning of the output frame.

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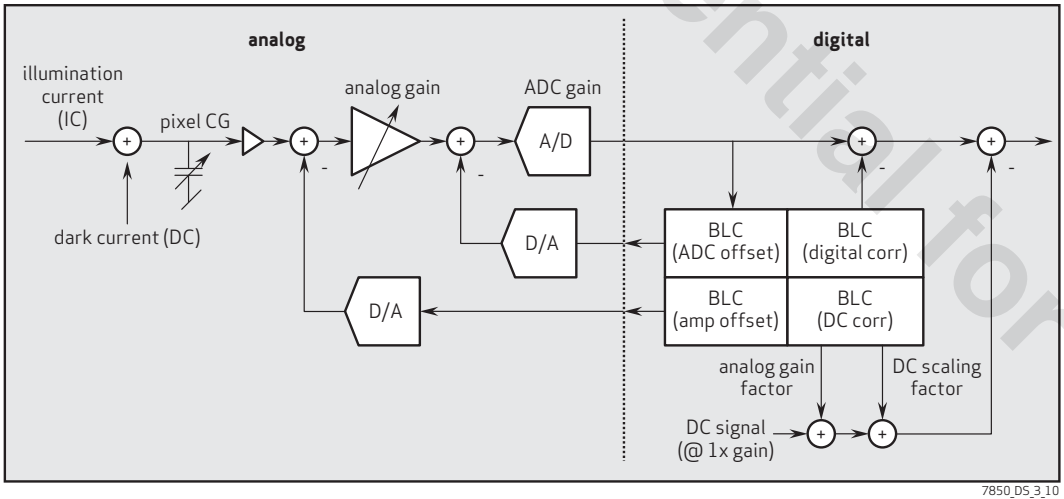
figure 3-10 BLC signal processing diagram



The signal processing flow for the BLC is shown in **figure 3-10**. The charge accumulated in the pixel during the exposure time is the sum of dark current (DC) and photon generated illumination current (IC). The accumulated charge is converted to a voltage signal in the pixel. The BLC controls two offset levels in the analog signal path, at the input and output of the analog gain amplifier. The correction in analog domain helps to optimize the utilization of the dynamic range of the amplifier and ADC. The remaining offset is subtracted in the digital domain to reach the target pedestal value. In order to compensate for systematic mismatch between the optical black and active pixel rows, a DC correction value can

be applied in digital domain. The BLC will measure the DC signal isolated at unity (1x) analog gain. This value is then multiplied with the a factor equivalent to the programmed analog gain and then multiplied with the DC scaling factor to compensate for the systematic mismatch between the optical black and the active pixels. The calculated DC correction value is then subtracted from the active pixel values. The correction can accommodate both systematic higher and lower DC signal in the optical black reference rows. The DC correction value for LPD is programmed in register 0x4035 and register 0x4036 for SPD. The measured DC signal for the three exposure channels are available in registers 0x4014 to 0x4019.

The BLC is based on measuring the value at the center of the distribution of the optical black reference pixels and applying analog and digital correction to bring the center to a predefined target value. The center of the pixel distribution is estimated from a combination of median and average filtering. The filtering for each BLC phase is based on 512 pixels from two optical black rows creating a total sample set of 1024 pixels. Only the values closest to the horizontal center of each row are used in order to minimize influence from any edge effects in the array. The four BLC phases are shown in **figure 3-11**.

BLC phase 1: Pixel conversion gain at target, analog gain set to unity (1x), pixel TX pulse suppressed, analog offset set to zero. The output from the optical black pixels represents the black level without dark current (DC).

BLC phase 2: Pixel conversion gain at target, analog gain set to unity (1x), pixel TX pulse active, analog offset set to zero. The output from the optical black pixels represents the black level with dark current (DC).

BLC phase 3: Pixel conversion gain at target, analog gain set to target, pixel TX pulse active, analog offset (amplifier) applied based on measurement from phase 2, analog offset (ADC) set to 0. The output from the optical black pixels represents the black level with dark current (DC) after pre-analog gain correction applied.

BLC phase 4: Pixel conversion gain at target, analog gain set to target, pixel TX pulse active, analog offset (amplifier) applied 2 and analog offset (ADC) applied based on measurement from phase 3. The output from the optical black pixels represents the black level with dark current (DC) after pre-and post-analog gain correction applied.

The output from phase 4 is used to estimate the digital correction value that is subtracted from the active pixel values. Also, the difference between phase 2 and phase 1 represents the dark current (DC) signal at unity gain. This value is then used for compensation of systematic mismatch between optical black and active pixels as described earlier in the chapter.

The output from the median and average filter is also used to estimate the variance of the dark current. The estimated variance is output through registers, but not used internally in the BLC.

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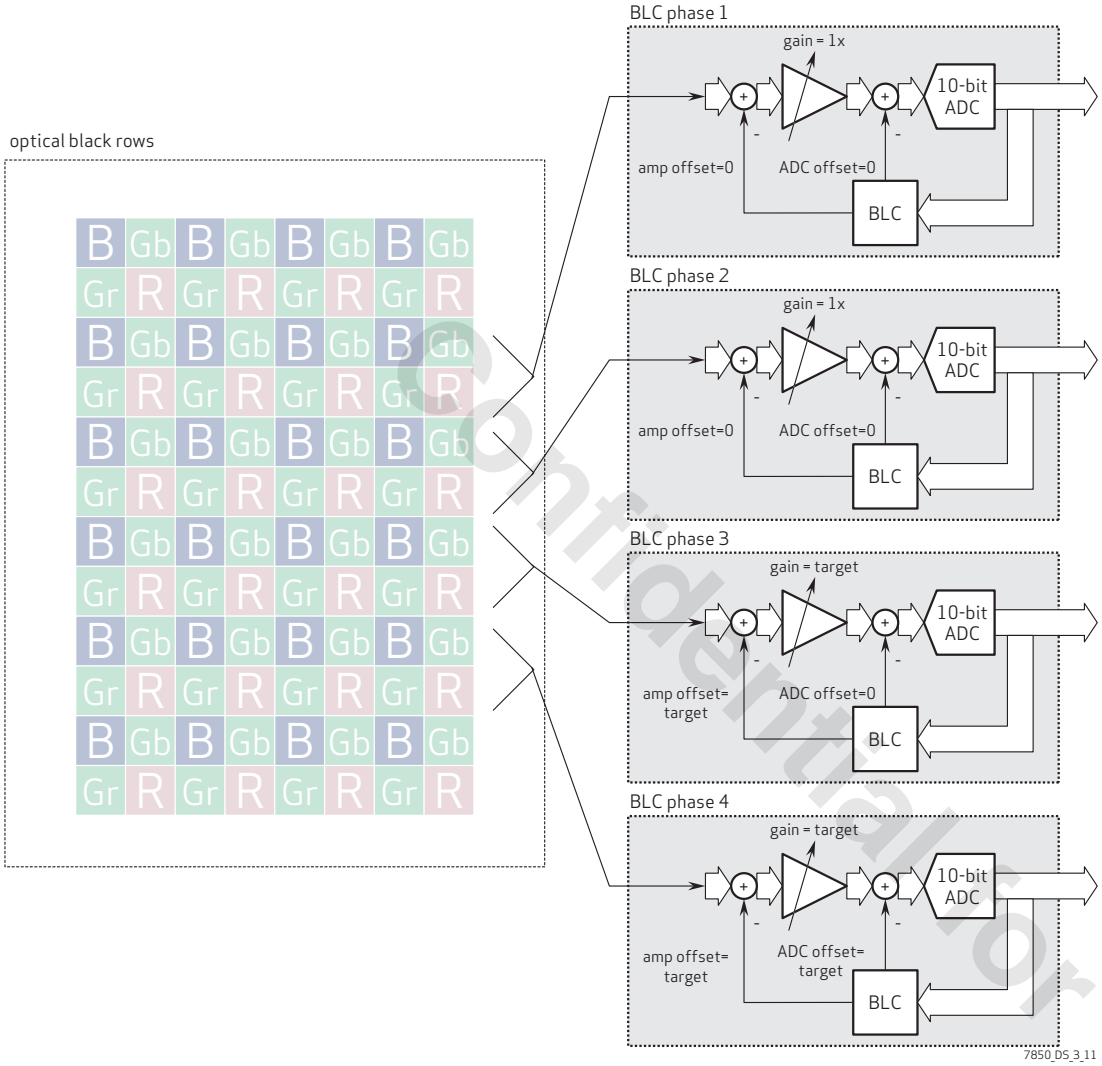
figure 3-11 BLC phase diagram



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The BLC algorithm can be re-triggered at various intervals (0x4002):

- every frame 0x4002[0]
- every frame with running average 0x4002[1]
- after coarse exposure time change 0x4002[3]
- after analog gain change 0x4002[2]
- from temperature measurement 0x4002[4]
- restart by register write 0x4002[5]

The number of frames with continuous updates after restart is programmable through register 0x4003.

The BLC supports operating in ABC mode by default. There is a 2 frame delay from the change of mode until the actual frame with these setting is generated:

To enable the filter operation on the digital offset correction, change the register 0x4002 to 0x0E. Note that if filter mode is enabled, the offset change re-trigger will not function and must be turned off.

To turn off re-trigger on the change of digital offset, change the register 0x4001 to 0x07.

The thresholds for re-trigger based on change of digital offsets are at 0x4037, 0x4038 and 0x4039.

table 3-3 BLC control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4000	BLC_CTRL0	0x75	RW	Bit[6]: Enable dig_offset_corr_s, S exposure When not enabled, register value will be used Bit[5]: Enable adc_offset_corr_s, S exposure When not enabled, register value will be used Bit[4]: Enable dac_offset_corr_s, S exposure When not enabled, register value will be used Bit[2]: Enable dig_offset_corr_l, L exposure When not enabled, register value will be used Bit[1]: Enable adc_offset_corr_l, L exposure When not enabled, register value will be used Bit[0]: Enable dac_offset_corr_l, L exposure When not enabled, register value will be used
0x4001	BLC_CTRL1	0x17	RW	Bit[4]: en_retrig_offset_change Bit[3]: Disable adc_corr_logic Used for test and debugging Bit[2]: Enable dig_offset_corr_vs, VS exposure When not enabled, register value will be used Bit[1]: Enable adc_offset_corr_vs, VS exposure When not enabled, register value will be used Bit[0]: Enable dac_offset_corr_vs, VS exposure When not enabled, register value will be used

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table 3-3 BLC control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4002	BLC_MODE	0x0E	RW	Bit[7]: Output filtered values of BLC calculations if enabled Bit[6]: Enable manual target adjustment from registers Bit[5]: Restart BLC Bit[4]: Enable automatic temperature change re-trigger Bit[3]: Enable automatic exposure change re-trigger Bit[2]: Enable automatic gain change re-trigger Bit[1]: Filter mode 1/4 new + 3/4 old value, affecting only dig_offset_corr Bit[0]: Updates every frame
0x4003	RESTART_FRAMES	0x01	RW	Bit[7:0]: Number of frames with continuous update after restart
0x4005	DAC_OFFSET_R_L	0x00	RW	Bit[4:0]: Use this value for L exposure, when dac_offset_corr is disabled
0x4006	DAC_OFFSET_R_S	0x00	RW	Bit[4:0]: Use this value for S exposure, when dac_offset_corr is disabled
0x4007	DAC_OFFSET_R_VS	0x00	RW	Bit[4:0]: Use this value for VS exposure, when dac_offset_corr is disabled
0x4008	ADC_OFFSET_R_L	0x00	RW	Bit[6:0]: Use this value for L exposure, when adc_offset_corr is disabled
0x4009	ADC_OFFSET_R_S	0x00	RW	Bit[6:0]: Use this value for S exposure, when adc_offset_corr is disabled
0x400A	ADC_OFFSET_R_VS	0x00	RW	Bit[6:0]: Use this value for VS exposure, when adc_offset_corr is disabled
0x400B	DIG_OFFSET_R_L	0x00	RW	Bit[7:0]: Use this value for L exposure, when dig_offset_corr is disabled
0x400C	DIG_OFFSET_R_S	0x00	RW	Bit[7:0]: Use this value for S exposure, when dig_offset_corr is disabled
0x400D	DIG_OFFSET_R_VS	0x00	RW	Bit[7:0]: Use this value for VS exposure, when dig_offset_corr is disabled
0x400E	BLC_TARGET_MAN_L_H	0x00	RW	Bit[1:0]: BLC target for L exposure when not in ISP mode[9:8] (manual_target_enable=1)
0x400F	BLC_TARGET_MAN_L_L	0x00	RW	Bit[7:0]: BLC target for L exposure when not in ISP mode[7:0] (manual_target_enable=1)

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table 3-3 BLC control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4010	BLC_TARGET_MAN_S_H	0x00	RW	Bit[1:0]: BLC target for S exposure when not in ISP mode[9:8] (manual_target_enable=1)
0x4011	BLC_TARGET_MAN_S_L	0x00	RW	Bit[7:0]: BLC target for S exposure when not in ISP mode[7:0] (manual_target_enable=1)
0x4012	BLC_TARGET_MAN_VS_H	0x00	RW	Bit[1:0]: BLC target for VS exposure when not in ISP mode[9:8] (isp_mode_n=1)
0x4013	BLC_TARGET_MAN_VS_L	0x00	RW	Bit[7:0]: BLC target for VS exposure when not in ISP mode[7:0] (isp_mode_n=1)
0x4014	DARK_CURRENT_L_H	–	R	Bit[1:0]: Measured dark current for L exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4015	DARK_CURRENT_L_L	–	R	Bit[7:0]: Measured dark current for L exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4016	DARK_CURRENT_S_H	–	R	Bit[1:0]: Measured dark current for S exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4017	DARK_CURRENT_S_L	–	R	Bit[7:0]: Measured dark current for S exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4018	DARK_CURRENT_VS_H	–	R	Bit[1:0]: Measured dark current for VS exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4019	DARK_CURRENT_VS_L	–	R	Bit[7:0]: Measured dark current for VS exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x401A	ROW_AVERAGE_01_L_H	–	R	Bit[3:0]: Average value for rows 0 and 1[11:8] L exposure, filter mode (1/4 new, 3/4 old), re-trigger overrides filter
0x401B	ROW_AVERAGE_01_L_L	–	R	Bit[7:0]: Average value for rows 0 and 1[7:0] L exposure, filter mode (1/4 new, 3/4 old), re-trigger overrides filter

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table 3-3 BLC control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x401C	ROW_AVERAGE_01_S_H	–	R	Bit[3:0]: Average value for rows 0 and 1 S exposure[11:8]
0x401D	ROW_AVERAGE_01_S_L	–	R	Bit[7:0]: Average value for rows 0 and 1 S exposure[7:0]
0x401E	ROW_AVERAGE_01_VS_H	–	R	Bit[3:0]: Average value for rows 0 and 1 VS exposure[11:8]
0x401F	ROW_AVERAGE_01_VS_L	–	R	Bit[7:0]: Average value for rows 0 and 1 VS exposure[7:0]
0x4020	ROW_AVERAGE_23_L_H	–	R	Bit[3:0]: Average value for rows 2 and 3 L exposure[11:8]
0x4021	ROW_AVERAGE_23_L_L	–	R	Bit[7:0]: Average value for rows 2 and 3 L exposure[7:0]
0x4022	ROW_AVERAGE_23_S_H	–	R	Bit[3:0]: Average value for rows 2 and 3 S exposure[11:8]
0x4023	ROW_AVERAGE_23_S_L	–	R	Bit[7:0]: Average value for rows 2 and 3 S exposure[7:0]
0x4024	ROW_AVERAGE_23_VS_H	–	R	Bit[3:0]: Average value for rows 2 and 3 VS exposure[11:8]
0x4025	ROW_AVERAGE_23_VS_L	–	R	Bit[7:0]: Average value for rows 2 and 3 VS exposure[7:0]
0x4026	ROW_AVERAGE_45_L_H	–	R	Bit[3:0]: Average value for rows 4 and 5 L exposure[11:8]
0x4027	ROW_AVERAGE_45_L_L	–	R	Bit[7:0]: Average value for rows 4 and 5 L exposure[7:0]
0x4028	ROW_AVERAGE_45_S_H	–	R	Bit[3:0]: Average value for rows 4 and 5 S exposure[11:8]
0x4029	ROW_AVERAGE_45_S_L	–	R	Bit[7:0]: Average value for rows 4 and 5 S exposure[7:0]
0x402A	ROW_AVERAGE_45_VS_H	–	R	Bit[3:0]: Average value for rows 4 and 5 VS exposure[11:8]
0x402B	ROW_AVERAGE_45_VS_L	–	R	Bit[7:0]: Average value for rows 4 and 5 VS exposure[7:0]
0x402C	ROW_AVERAGE_67_L_H	–	R	Bit[3:0]: Average value for rows 6 and 7 L exposure[11:8]
0x402D	ROW_AVERAGE_67_L_L	–	R	Bit[7:0]: Average value for rows 6 and 7 L exposure[7:0]
0x402E	ROW_AVERAGE_67_S_H	–	R	Bit[3:0]: Average value for rows 6 and 7 S exposure[11:8]

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table 3-3 BLC control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x402F	ROW_AVERAGE_67_S_L	–	R	Bit[7:0]: Average value for rows 6 and 7 S exposure[7:0]
0x4030	ROW_AVERAGE_67_VS_H	–	R	Bit[3:0]: Average value for rows 6 and 7 VS exposure[11:8]
0x4031	ROW_AVERAGE_67_VS_L	–	R	Bit[7:0]: Average value for rows 6 and 7 VS exposure[7:0]
0x4032	DAC_OFFSET_STEP	0x0D	RW	Bit[7:0]: DAC offset step
0x4033	DAC_OFFSET_BIAS	0x14	RW	Bit[7:0]: DAC offset bias Subtracted before division
0x4034	CLK_RATIO	0x80	RW	Bit[7:0]: Ratio (ADC_CLK×2)/(SCLK3X) format 3.5
0x4035	D_VALUE_L_VS	0x00	RW	Bit[5]: Sign (S) Bit[4:0]: Value (xyzuv) -/+ (S) 0.0x40yzuv is used to equalize dark current for visual and dark pixels
0x4036	D_VALUE_S	0x00	RW	Bit[5]: Sign (S) Bit[4:0]: Value (xyzuv) -/+ (S) 0.0x40yzuv is used to equalize dark current for visual and dark pixels
0x4037	OFFSET_THRES_L	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x4038	OFFSET_THRES_S	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x4039	OFFSET_THRES_VS	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x403A	N_TARGET_BIAS_L	0x00	RW	Bit[7:0]: Bias for ADC offset L
0x403B	N_TARGET_BIAS_S	0x00	RW	Bit[7:0]: Bias for ADC offset S
0x403C	N_TARGET_BIAS_VS	0x00	RW	Bit[7:0]: Bias for ADC offset VS
0x4040	VARIANCE_L_H	–	R	Bit[7:0]: Variance dark current, L exposure[15:8]
0x4041	VARIANCE_L_L	–	R	Bit[7:0]: Variance dark current, L exposure[7:0]
0x4042	VARIANCE_S_H	–	R	Bit[7:0]: Variance dark current, S exposure[15:8]
0x4043	VARIANCE_S_L	–	R	Bit[7:0]: Variance dark current, S exposure[7:0]

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table 3-3 BLC control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x4044	VARIANCE_VS_H	–	R	Bit[7:0]: Variance dark current, VS exposure[15:8]
0x4045	VARIANCE_VS_L	–	R	Bit[7:0]: Variance dark current, VS exposure[7:0]
0x4046	COL_AMP_OFS_L	–	R	Bit[4:0]: BLC calculated DAC value for L exposure
0x4047	COL_AMP_OFS_S	–	R	Bit[4:0]: BLC calculated DAC value for S exposure
0x4048	COL_AMP_OFS_VS	–	R	Bit[4:0]: BLC calculated DAC value for VS exposure
0x4049	N_TARGET_L	–	R	Bit[7:0]: BLC calculated ADC correction value for L exposure
0x404A	N_TARGET_S	–	R	Bit[7:0]: BLC calculated ADC correction value for S exposure
0x404B	N_TARGET_VS	–	R	Bit[7:0]: BLC calculated ADC correction value for VS exposure
0x404C	DIG_OFFSET_L	–	R	Bit[7:0]: BLC calculated digital offset value for L exposure
0x404D	DIG_OFFSET_S	–	R	Bit[7:0]: BLC calculated digital offset value for S exposure
0x404E	DIG_OFFSET_VS	–	R	Bit[7:0]: BLC calculated digital offset value for VS exposure

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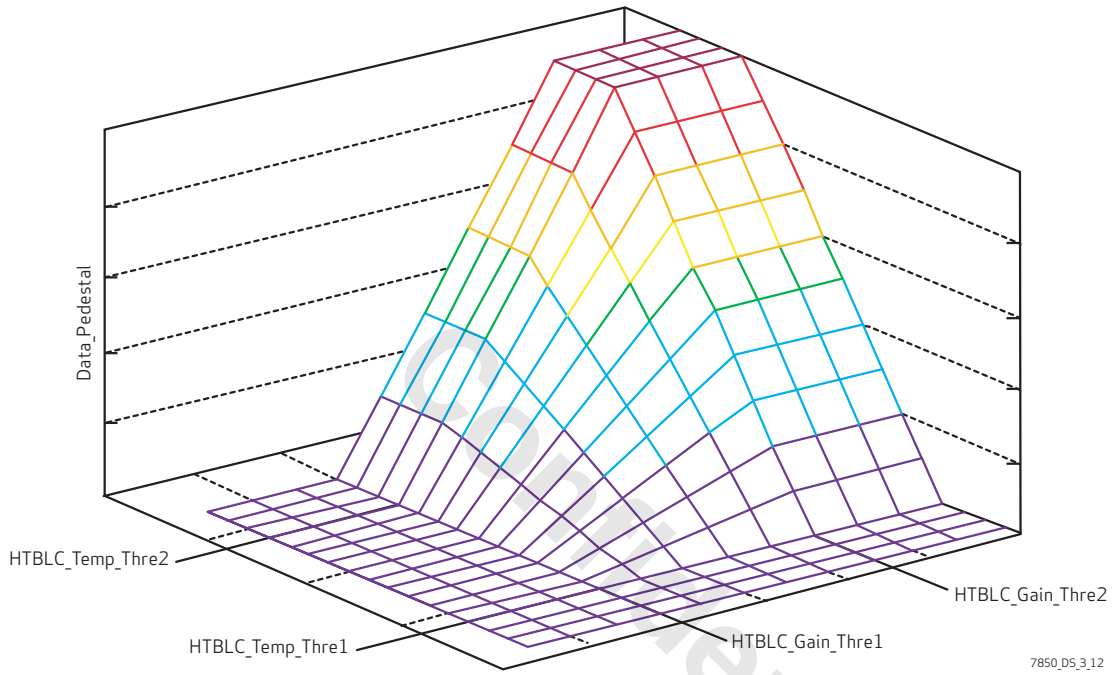
3.7.1 BLC control at high temperature

At high temperature, the dark current across the pixel array is not uniform due to uneven heat generation. To mitigate the unevenness and reduce signal cutoff in low dark current area, the OV7850 implements an option to automatically increase the data pedestal value with temperature and analog gain or dark current and analog gain. Here, temperature is read back from the temperature sensor and dark current is read back from dark row value. This function is enabled by register 0x5A12[0]. When 0x550C[3] is 1, the data pedestal value is dependent on dark current and temperature. The maximum increment of the long and short channel pedestals are set by registers 0x5A13 and 0x5A14, respectively. The gain threshold to start the adjustment is set by registers {0x5A0E, 0x5A0F}, and the threshold reaching the maximum adjustment is set by registers {0x5A10, 0x5A11}. Similarly, the temperature threshold to start the adjustment is set by register 0x5A0C. The threshold reaching the maximum adjustment is set by register 0x5A0D. The dark current threshold to start the adjustment is set by registers {0x5A20, 0x5A21}. The dark current reaching the maximum adjustment is set by registers {0x5A22, 0x5A23} (see **figure 3-12**).

figure 3-12 BLC at high temperature diagram



When the data pedestal adjustment at high temperature is enabled, the data pedestal that the ISP subtracted should stay unchanged to mitigate the unevenness.

3.7.2 gamma control at high temperature

The side effect of increasing data pedestal is the color bias caused by the remaining dark current. Another way to reduce the unevenness is to reduce digital gain by decreasing gamma. This function is enabled by register 0x5A16. HDR gamma is real gamma, which will dramatically amplify the lower signal. This will cause the unevenness to be amplified.

Refer to **figure 3-13** for the gamma reduction curve with temperature. Gamma_Thre1 is set by register 0x5A17, Gamma_Thre2 is set by register 0x5A18. When temperature reaches threshold Temp_Thre1(0x5A0C), the gamma will start to decrease. When the temperature reaches the threshold Temp_Thre2(0x5A0D), the gamma will decrease to Gamma_Thre2.

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figure 3-13 gamma reduction curve

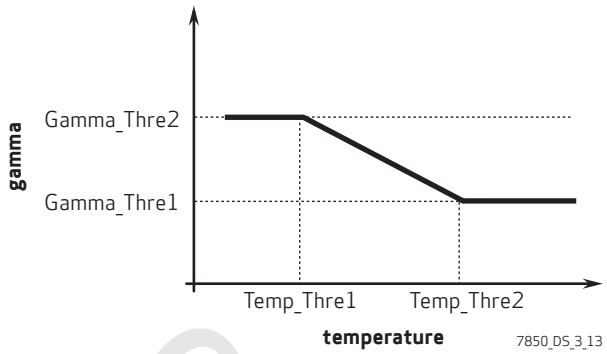

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table 3-4 high temperature BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x550C	HT_ISP	0x09	RW	Bit[3]: Dark current and gain based BLC compensation Bit[2]: New night mode enable Bit[1:0]: Reserved
0x5A0C	HTBLC_TEMP_THRE1	0x46	RW	High Temperature BLC Temperature Start Threshold
0x5A0D	HTBLC_TEMP_THRE2	0x64	RW	High Temperature BLC Temperature End Threshold
0x5A0E	HTBLC_GAIN_THRE1_H	0x00	RW	High Temperature BLC Analog Gain Start Threshold, High Byte
0x5A0F	HTBLC_GAIN_THRE1_L	0x80	RW	High Temperature BLC Analog Gain Start Threshold, Low Byte
0x5A10	HTBLC_GAIN_THRE2_H	0x01	RW	High Temperature BLC Analog Gain End Threshold, High Byte
0x5A11	HTBLC_GAIN_THRE2_L	0x00	RW	High Temperature BLC Analog Gain End Threshold, Low Byte
0x5A12	HT_BLCOFFSETENABLE	0x00	RW	High Temperature BLC Target Offset Enable When register value is 0, function is disabled. Other values mean enabled.
0x5A13	HT_MAX_BLCOFFSET_L	0x70	RW	High Temperature BLC Target Offset BLC Offset for Long Exposure
0x5A14	HT_MAX_BLCOFFSET_S	0x30	RW	High Temperature BLC Target Offset BLC Offset for Short Exposure

table 3-4 high temperature BLC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5A15	HT_MAX_BLCOFFSET_VS	0x10	RW	High Temperature BLC Target Offset BLC Offset for VS Exposure
0x5A16	HT_GAMMAENABLE	0x01	RW	High Temperature BLC Limit Gamma Function Enable When register value is 0, function is disabled. Other values mean enabled.
0x5A17	HT_GAMMATHRE1	0x04	RW	High Temperature BLC Limit Minimum Gamma Threshold
0x5A18	HT_GAMMATHRE2	0x08	RW	High Temperature BLC Limit Maximum Gamma Threshold
0x5A20	HT_DARKCURRENTTHRE1_H	0x00	RW	High Temperature BLC Dark Current Start Threshold, High Byte
0x5A21	HT_DARKCURRENTTHRE1_L	0x10	RW	High Temperature BLC Dark Current Start Threshold, Low Byte
0x5A22	HT_DARKCURRENTTHRE2_H	0x00	RW	High Temperature BLC Dark Current End Threshold, High Byte
0x5A23	HT_DARKCURRENTTHRE2_L	0xA0	RW	High Temperature BLC Dark Current End Threshold, Low Byte

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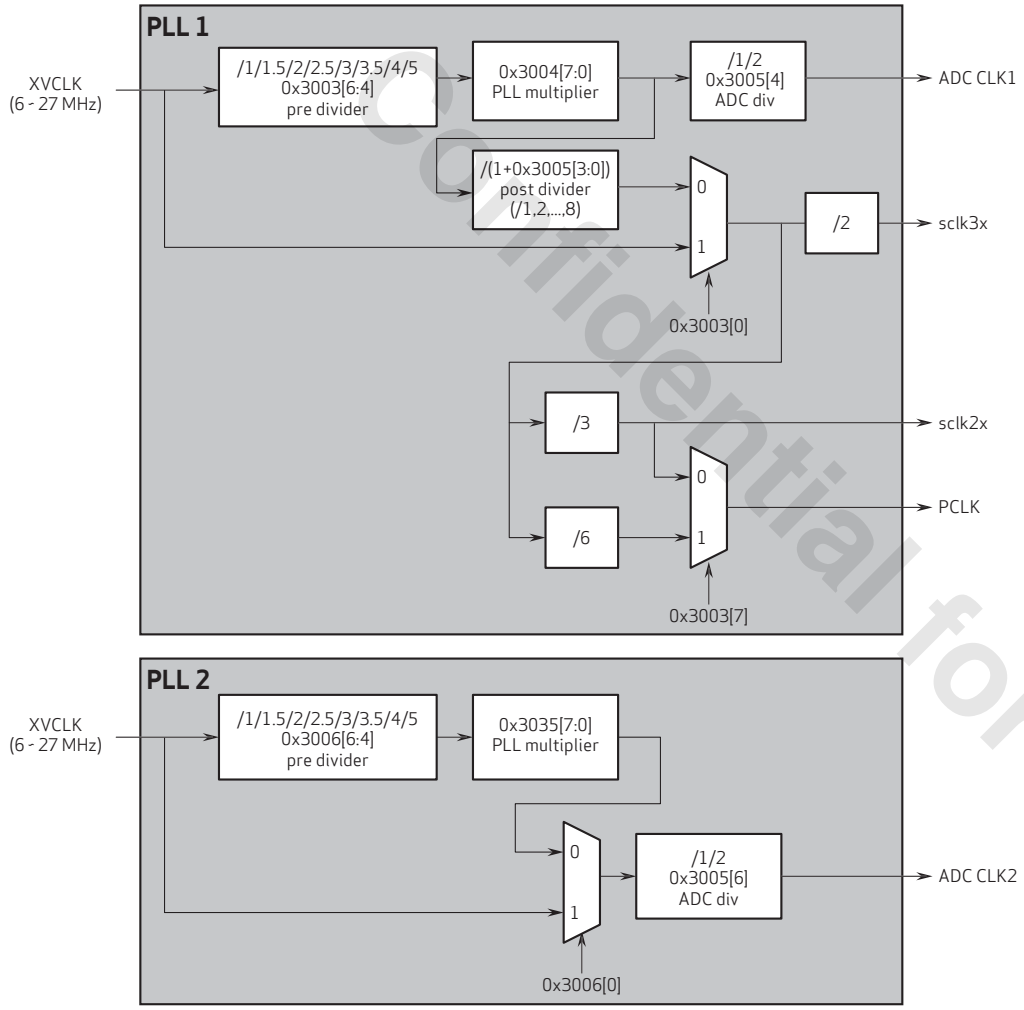
3.8 PLL and clock tree

figure 3-14 shows the structure of the on-chip PLLs that are used to generate the required clock signals. PLL1 is used to generate two internal system clocks (sclk3x, sclk2x), the pixel clock (PCLK) and an internal reference clock (ADC CLK1), which is used by the ADC. Alternatively, PLL2 can be used to generate the reference clock signal (ADC CLK2) for the ADC. All clock signals are derived from the 6-27MHz input reference clock XVCLK. PLL settings can only be changed during sensor standby mode (0x303E = 0).

figure 3-14 PLL control diagram



note 1 reference frequency range after XVCLK pass through pre divider: 3-27MHz

note 2 VCO frequency range after clock pass through pll multiplier: 200-500MHz

note 3 limitation for PLL multiplier: 1-256

note 4 PLL clock must be configured in standby mode

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table 3-5 SC_CMMN control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3000	PAD_OEN0	0x00	RW	Bit[7:0]: Pad output enable 0
0x3001	PAD_OEN1	0x00	RW	Bit[7:0]: Pad output enable 1
0x3002	PAD_OEN2	0x00	RW	Pad Output Enable 2 Bit[7]: VSYNC output enable Bit[6]: HREF output enable Bit[5]: PCLK output enable
0x3003	PLL_CTRL0	0x24	RW	Bit[7]: pll1_pclk_sel Bit[6:4]: pll1_prediv Bit[3:1]: Reserved Bit[0]: pll1_bypass
0x3004	PLL_CTRL1	0x24	RW	Bit[7:0]: pll1_plldiv
0x3005	PLL_CTRL2	0x51	RW	Bit[7]: pll2_div_rst Bit[6]: pll2_dacdiv Bit[5]: pll1_div_rst Bit[4]: pll1_dacdiv Bit[3:0]: pll1_sysdiv
0x3006	PLL_CTRL3	0x22	RW	Bit[7]: pll2_enable Bit[6:4]: pll2_prediv Bit[3:1]: Reserved Bit[0]: pll2_bypass
0x3007	PCLK_DIV_CTRL	0x00	RW	Bit[7]: Reserved Bit[3:0]: pclk_div
0x3008	PAD_OUT0	0x00	RW	Bit[7:0]: io_y_o[15:8]
0x3009	PAD_OUT1	0x00	RW	Bit[7:0]: io_y_o[7:0]
0x300A	CHIP_ID_H	0xA6	R	Bit[7:0]: Chip ID high byte
0x300B	CHIP_ID_L	0x26	R	Bit[7:0]: Chip ID low byte
0x300C	SCCB_ID	0x60	RW	Bit[7:1]: sccb_id_n Bit[0]: sccb_id_sel 0: {sccb_id[7:4],gpio_i[3:1]} 1: sccb_id[7:1]
0x300D	PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: io_pclk_o Bit[4:0]: Reserved
0x300E	PAD_SEL0	0x00	RW	Bit[7:0]: io_y_sel[15:8]
0x300F	PAD_SEL1	0x00	RW	Bit[7:0]: io_y_sel[7:0]

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table 3-5 SC_CMMN control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3010	PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: io_pclk_sel Bit[4:0]: Reserved
0x3011	A_PAD_PK	0x02	RW	Bit[7:6]: ip2x3v 00: 1x driving capability 01: 2x driving capability 10: 3x driving capability 11: 4x driving capability Bit[2]: pll_rst 0: Release PLL reset 1: Reset PLLs
0x3012	SENSOR_GATE_CTRL_H	0xFF	RW	Bit[7]: Sensor gate BLC enable Bit[6]: Sensor gate ISP enable Bit[5]: Sensor gate ISP2X enable Bit[4]: Sensor gate VFIFO enable Bit[3]: Sensor gate DVP enable Bit[0]: Sensor gate OTP enable
0x3016~ 0x3023	RSVD	–	–	Reserved
0x3024	CORE_CTRL1_H	0x80	RW	Bit[7]: Enables YUV in 8-bit mode Bit[6:4]: raw_modes 000: RAW 10 bits 001: RAW 8 bits 010: RAW 16 bits 100: RAW 18 bits 110: RAW 20 bits
0x3025	CORE_CTRL1_L	0x00	RW	Bit[5]: fsin_out 0: Not used 1: Sensor generated frame sync goes to pad FSIN Bit[4]: c_fsin 0: Pad is input (FSIN) 1: Pad FSIN is output Bit[0]: en_arb0_timeout
0x302A~ 0x302E	RSVD	–	–	Reserved
0x302F	GPIO01	0x22	RW	Bit[7]: gpio1_out Bit[6]: gpio1_dir Bit[5:4]: gpio1_sel Bit[3]: gpio0_out Bit[2]: gpio0_dir Bit[1:0]: gpio0_sel
0x3030~ 0x3034	RSVD	–	–	Reserved

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table 3-5 SC_CMMN control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3035	PLL_CTRL4	0x1C	RW	Bit[7:0]: PLL control
0x3036	GPIO01_2	–	R	Bit[7:5]: Reserved Bit[4]: gpio0_in (read only) Bit[3:1]: Reserved Bit[0]: gpio1_in (read only)
0x3038	MAN_ID_H	–	R	Bit[7:0]: Manufacture ID high byte
0x3039	MAN_ID_L	–	R	Bit[7:0]: Manufacture ID low byte
0x303A	SLP_CNT_H	–	R	SLP_CNT_H
0x303B	SLP_CNT_L	–	R	SLP_CNT_L
0x303E	SOFTWARE_ CTRL1	0x00	RW	Bit[4:1]: Reserved Bit[0]: sfw_stb 0: Software standby 1: Streaming
0x303F	SOFTWARE_ CTRL2	0x04	RW	Bit[2]: Power-down standby option 0: Power-down system with sfw_stb 1: Power-down system without sfw_stb Bit[1]: Software standby immediately when this bit is set Bit[0]: Software reset
0x3040~ 0x3048	RSVD	–	–	Reserved

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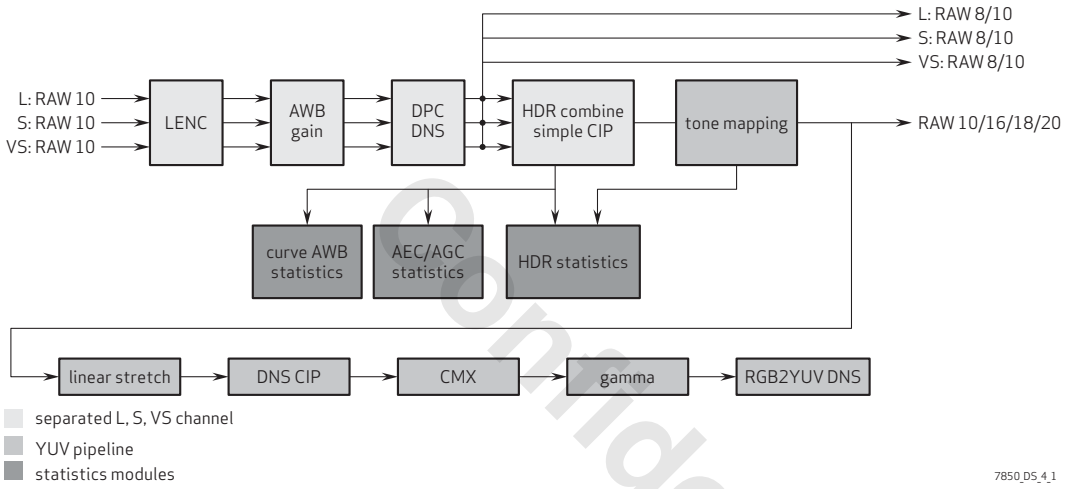
4 image processor

figure 4-1 shows the top level block diagram of the OV7850 image processor.

figure 4-1 image processor block diagram



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The image processor pipeline (ISP) receives image data from the sensor core. The video stream arrives as 10-bit parallel data separated in long exposure (L), short exposure (S) and very short exposure (VS) channel. Unused rows and columns are cut before further processing. One of the first processing steps in the ISP is to correct the shading caused by lens fall off (LENC). Digital gain is then applied to make the image white balanced (AWB gain). Defect pixel and clusters (DPC) are corrected on-the-fly for each exposure channel.

Before the exposure channels are combined (HDR combine), they are processed through a noise filter (DNS). RAW 8/10 for separated exposure channels can be output from here. Then a simple color interpolation is then applied. The image data in the dark area of the HDR image is from the L channel, while the data in the bright area is from the S and VS channel. In the transition area, the data is linearly combined. The weighting used in the combination feeds back to the AEC/AGC, HDR and AWB block to calculate the statistics.

Tone mapping is applied to compress the dynamic range of the full 30-bit representation to output combined RAW 10/16/18/20. The combined RAW10 data used further down streams in the YUV pipeline data is stretched to enhance the contrast of the image.

Color interpolation (CIP) recovers the missing color channels of each pixel from the neighboring pixels. To reduce noise and enhance edges the video data noise and sharpness filter is applied. A color correction matrix (CMX) is applied on the R, G and B values of each pixel to improve the color fidelity due to spectrum crosstalk.

A global gamma correction is applied to the image to further improve the image rendering. The image data is sent via a formatter block to the output interface.

- If ISP is disabled (0x5000[0]), the following modules will be disabled: LENC, AWB, DPC, DNS, tone mapping, linear stretch, CIP, CMX, gamma, RGB2YUV. Statistics modules and related data-path modules, such as simple CIP, advanced AWB, combine, AEC_AGC and HDR statistic, can still be available if its enable signals are active.
- If output format is RAW, all YUV processing modules will be automatically be disabled.
- If long exposure mode is enabled, combine, tone mapping and HDR statistic will be disabled.

table 4-1 ISP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	R_ISP_CTRL_0	0xFB	RW	Bit[7]: AEC/AGC enable Bit[6]: Combine enable Bit[5]: Curve WB/manual WB enable 0: Manual WB enable 1: Curve WB enable Bit[4]: Simple interpolation enable Bit[3]: HDR RAW DNS enable Bit[2]: LENC enable Bit[1]: AWB gain enable Bit[0]: ISP enable
0x5001	R_ISP_CTRL_1	0xDF	RW	Bit[7]: OVPB CIP PAD enable Bit[6]: OVPB CIP enable Bit[5]: OVPB RAW DNS enable Bit[4]: Reserved Bit[3]: DPC enable Bit[2]: Linear stretch enable Bit[1]: Log enable Bit[0]: Tone mapping enable
0x5002	R_ISP_CTRL_2	0x7F	RW	Bit[7]: Make virtual long enable Bit[6]: UVDNS enable Bit[5]: HDR statistic enable Bit[4]: ISP sub-module clock global enable Bit[3]: RGB2YUV enable Bit[2]: Reserved Bit[1]: Gamma enable Bit[0]: CMX enable
0x5003	R_ISP_CTRL_3	0xB0	RW	Bit[7]: ISP output window crop enable (active high) Bit[6]: ISP input window crop enable (active high) Bit[5]: OVPB buffer auto dummy line enable Bit[4]: HDR buffer auto dummy line enable Bit[3:2]: ISP EOF signal select Bit[1:0]: CFA pattern
0x5004~ 0x5006	RSVD	–	–	Reserved

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table 4-1 ISP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5007	R_ISP_CTRL_7	0x00	RW	Bit[7]: ISP output RAW10 selection 0: Non-combined RAW 10 1: Combined RAW10 Bit[6]: Manual sensor option enable Bit[5]: Manual sensor mirror option Bit[4]: Manual sensor flip option Bit[3:2]: Manual sensor X skip Bit[1:0]: Manual sensor Y skip
0x5008	R_ISP_CTRL_8	0x00	RW	Bit[1:0]: Manual sensor X offset[9:8]
0x5009	R_ISP_CTRL_9	0x00	RW	Bit[7:0]: Manual sensor X offset[7:0]
0x500A	R_ISP_CTRL_A	0x00	RW	Bit[1:0]: Manual sensor Y offset[9:8]
0x500B	R_ISP_CTRL_B	0x00	RW	Bit[7:0]: Manual sensor Y offset[7:0]
0x500C	R_ISP_CTRL_C	0x00	RW	Bit[1:0]: Target BLC for long[9:8]
0x500D	R_ISP_CTRL_D	0x10	RW	Bit[7:0]: Target BLC for long[7:0]
0x500E	R_ISP_CTRL_E	0x00	RW	Bit[1:0]: Target BLC for short[9:8]
0x500F	R_ISP_CTRL_F	0x10	RW	Bit[7:0]: Target BLC for short[7:0]
0x5010	R_ISP_CTRL_10	0x00	RW	Bit[1:0]: Target BLC for vshort[9:8]
0x5011	R_ISP_CTRL_11	0x10	RW	Bit[7:0]: Target BLC for vshort[7:0]
0x5012	R_ISP_CTRL_12	0x00	RW	Bit[1:0]: ISP input window crop X direction (horizontal) start coordinate[9:8]
0x5013	R_ISP_CTRL_13	0x00	RW	Bit[7:0]: ISP input window crop X direction (horizontal) start coordinate[7:0]
0x5014	R_ISP_CTRL_14	0x00	RW	Bit[1:0]: ISP input window crop Y direction (vertical) start coordinate[9:8]
0x5015	R_ISP_CTRL_15	0x00	RW	Bit[7:0]: ISP input window crop Y direction (vertical) start coordinate[7:0]
0x5016	R_ISP_CTRL_16	0x02	RW	Bit[1:0]: ISP input window crop module output width[9:8]
0x5017	R_ISP_CTRL_17	0xF0	RW	Bit[7:0]: ISP input window crop module output width[7:0]
0x5018	R_ISP_CTRL_18	0x02	RW	Bit[1:0]: ISP input window crop module output height[9:8]
0x5019	R_ISP_CTRL_19	0x08	RW	Bit[7:0]: ISP input window crop module output height[7:0]
0x501A~ 0x501D	RSVD	–	–	Reserved

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table 4-1 ISP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x501E	R_ISP_CTRL_1E	0x00	RW	Bit[7]: HDR buffer manual control enable Bit[6]: OVPB buffer manual control enable Bit[5]: HDR buffer manual enable Bit[4]: OVPB buffer manual enable Bit[3:2]: RGB2YUV bypass channel select 0x: G channel 10: B channel 11: R channel Bit[1]: HDR buffer control dummy line manual HREF blank cycles enable Bit[0]: OVPB buffer control dummy line manual HREF blank cycles enable
0x501F	R_PRE_CTRL0	0x00	RW	Bit[7]: Test pattern enable (active high) Bit[6]: Rolling effect enable (active high) Bit[5]: Transparent effect enable (active high) Bit[4]: Not used Bit[3:2]: Color bar style select Bit[1:0]: Test pattern select 00: Color bar Others: Not used
0x5020~ 0x5027	RSVD	–	–	Reserved

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4.1 test pattern

For testing purposes, the OV7850 offers analog and digital test patterns. The analog test pattern is a color bar as an overlay image (test pattern applied on pixel output to exercise the whole analog readout channel) and is enabled by setting register 0x3613[4]=1. The intensity of this color-bar can be control by register 0x3613[3:0] and you can also swap the order of the colors by setting register 0x3613[5]=1. The digital test patterns include color bar in different styles, including transparent and rolling bar effect. The digital test pattern function is enabled by register 0x501F[7] and the test pattern is selected by register 0x501F[6:0].

4.1.1 color bar

There are four types of color bars shown in **figure 4-2** selected from register 0x501F.

figure 4-2 color bar types

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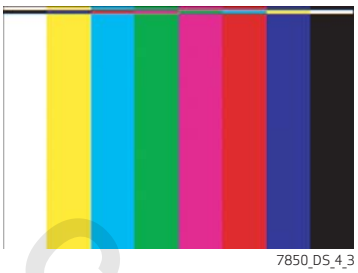
4.1.2 rolling bar effect

Rolling bar on color bar image is selected by register 0x501F[6].

figure 4-3 rolling bar effect



Since the digital test patterns passes through the pipeline, to get a consistent output pattern, a number of processing steps needs to be stopped before enabling the test pattern. Please contact your local OmniVision FAE to get a valid setting file.

table 4-2 test pattern registers

address	register name	default value	R/W	description
0x3013	SREG19	0x08	RW	Bit[5]: Color bar swap order of colors Bit[4]: Color bar enable overlay on output image Bit[3:0]: Color bar amplitude adjustment
0x501F	R_PRE_CTRL0	0x00	RW	Bit[7]: Test pattern enable (active high) Bit[6]: Rolling effect enable (active high) Bit[5]: Transparent effect enable (active high) Bit[4]: Not used Bit[3:2]: Color bar style select Bit[1:0]: Test pattern select 00: Color bar Others:Not Used
0x5021	RSVD	–	–	Reserved

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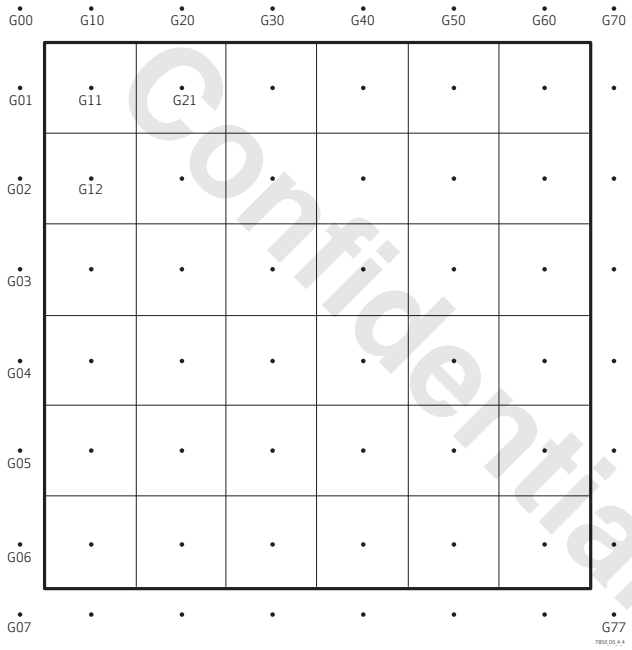
4.2 lens correction (LENC)

The first step in the image processing pipeline is to correct the shading due to light fall off in the edges and corner areas. The correction is done by multiplying each pixel with a gain based on the area where each pixel is located. The gain to apply is calculated from a 8x8 grid with control points for both luminance (G) and each color channel (B, R) separately. The control points are separated for LPD (L,VS) and SPD (S), see registers 0x5200~0x537F. LENC is disabled by default and can be enabled by register 0x5000[2].

figure 4-4 LENC control points



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The control points are selected according to the absolute coordinate of the input pixel in the sensor array. In other words, if y_offset and x_offset are bigger than 0 (0x3800~0x3803 value are bigger than 0), the control point (0,0) can not be used, or if image is flipped, control points will be selected from the back. The control points are located in the center of each sub-array and contain data on the lens artifacts in their respective locations in the pixel array.

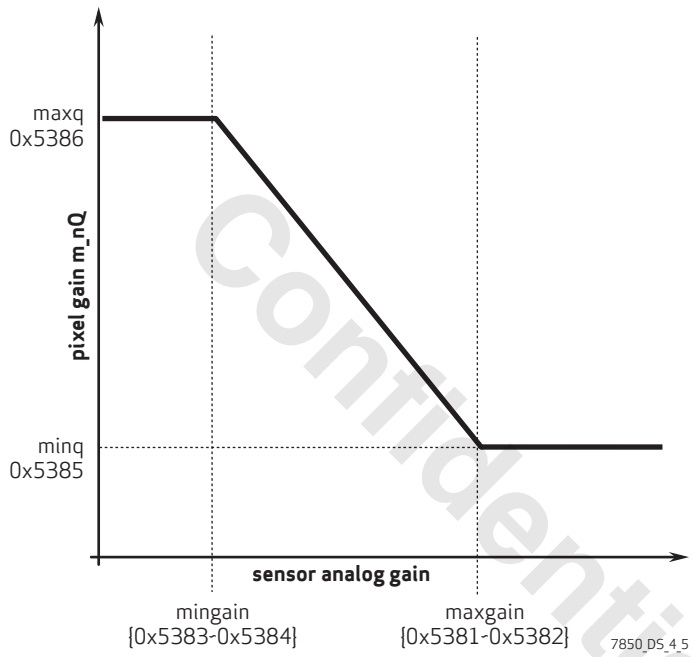
The OV7850 supports sub-sampling and flip in both horizontal and vertical directions while LENC is enabled.

The LENC control registers are separate for L, S and VS exposure. The following explanation is for L/VS, please see **table 4-3** for S.

Under dark conditions, the signal-to-noise ratio (SNR) drops in the corner areas. The noise can be significantly amplified by the lens correction gain and results in a brighter corner. The OV7850 can automatically adjust gain for the pixels to adapt to lighting conditions (m_nQ). This is accomplished by following the sensor analog gain and is enabled through register 0x5380[0] for LPD (enabled by default). If register 0x5380[0] is clear, LENC gain is fixed.

When scene brightness increases, the sensor analog gain decrease towards its minimum (mingain) and correspondingly, the LENC gain increases towards its maximum (maxq), see **figure 4-5**. When scene brightness decreases, the sensor analog gain increases towards its maximum (maxgain), and the LENC gain decreases towards its minimum (minq).

figure 4-5 lens correction graph



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Note that, L/S/VS channel can share the same value of m_nQ calculated by L channel. The 8x8 control point matrix are however independent for L/VS (LPD) and S (SPD) channel correspondingly.

By setting register 0x5380[3], the lens correction gain adjustments use the same luminance compensation level from L channel to apply it on L,S and VS channels.

The luminance compensation levels used can be read from registers 0x53A9~0x53AB.

LENC control point parameters must be calibrated with a specific tool, please contact your regional OmniVision FAE for assistance.

table 4-3 LENC control registers (sheet 1 of 18)

address	register name	default value	R/W	description
0x5200	LENC_L_G00	0x00	RW	Bit[5:0]: G00 of 8x8 G control point array for L/VS
0x5201	LENC_L_G01	0x00	RW	Bit[5:0]: G01 of 8x8 G control point array for L/VS

table 4-3 LENC control registers (sheet 2 of 18)

address	register name	default value	R/W	description
0x5202	LENC_L_G02	0x00	RW	Bit[5:0]: G02 of 8x8 G control point array for L/VS
0x5203	LENC_L_G03	0x00	RW	Bit[5:0]: G03 of 8x8 G control point array for L/VS
0x5204	LENC_L_G04	0x00	RW	Bit[5:0]: G04 of 8x8 G control point array for L/VS
0x5205	LENC_L_G05	0x00	RW	Bit[5:0]: G05 of 8x8 G control point array for L/VS
0x5206	LENC_L_G06	0x00	RW	Bit[5:0]: G06 of 8x8 G control point array for L/VS
0x5207	LENC_L_G07	0x00	RW	Bit[5:0]: G07 of 8x8 G control point array for L/VS
0x5208	LENC_L_G10	0x00	RW	Bit[5:0]: G10 of 8x8 G control point array for L/VS
0x5209	LENC_L_G11	0x00	RW	Bit[5:0]: G11 of 8x8 G control point array for L/VS
0x520A	LENC_L_G12	0x00	RW	Bit[5:0]: G12 of 8x8 G control point array for L/VS
0x520B	LENC_L_G13	0x00	RW	Bit[5:0]: G13 of 8x8 G control point array for L/VS
0x520C	LENC_L_G14	0x00	RW	Bit[5:0]: G14 of 8x8 G control point array for L/VS
0x520D	LENC_L_G15	0x00	RW	Bit[5:0]: G15 of 8x8 G control point array for L/VS
0x520E	LENC_L_G16	0x00	RW	Bit[5:0]: G16 of 8x8 G control point array for L/VS
0x520F	LENC_L_G17	0x00	RW	Bit[5:0]: G17 of 8x8 G control point array for L/VS
0x5210	LENC_L_G20	0x00	RW	Bit[5:0]: G20 of 8x8 G control point array for L/VS
0x5211	LENC_L_G21	0x00	RW	Bit[5:0]: G21 of 8x8 G control point array for L/VS
0x5212	LENC_L_G22	0x00	RW	Bit[5:0]: G22 of 8x8 G control point array for L/VS
0x5213	LENC_L_G23	0x00	RW	Bit[5:0]: G23 of 8x8 G control point array for L/VS
0x5214	LENC_L_G24	0x00	RW	Bit[5:0]: G24 of 8x8 G control point array for L/VS
0x5215	LENC_L_G25	0x00	RW	Bit[5:0]: G25 of 8x8 G control point array for L/VS
0x5216	LENC_L_G26	0x00	RW	Bit[5:0]: G26 of 8x8 G control point array for L/VS
0x5217	LENC_L_G27	0x00	RW	Bit[5:0]: G27 of 8x8 G control point array for L/VS
0x5218	LENC_L_G30	0x00	RW	Bit[5:0]: G30 of 8x8 G control point array for L/VS
0x5219	LENC_L_G31	0x00	RW	Bit[5:0]: G31 of 8x8 G control point array for L/VS
0x521A	LENC_L_G32	0x00	RW	Bit[5:0]: G32 of 8x8 G control point array for L/VS
0x521B	LENC_L_G33	0x00	RW	Bit[5:0]: G33 of 8x8 G control point array for L/VS
0x521C	LENC_L_G34	0x00	RW	Bit[5:0]: G34 of 8x8 G control point array for L/VS
0x521D	LENC_L_G35	0x00	RW	Bit[5:0]: G35 of 8x8 G control point array for L/VS

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table 4-3 LENC control registers (sheet 3 of 18)

address	register name	default value	R/W	description
0x521E	LENC_L_G36	0x00	RW	Bit[5:0]: G36 of 8x8 G control point array for L/VS
0x521F	LENC_L_G37	0x00	RW	Bit[5:0]: G37 of 8x8 G control point array for L/VS
0x5220	LENC_L_G40	0x00	RW	Bit[5:0]: G40 of 8x8 G control point array for L/VS
0x5221	LENC_L_G41	0x00	RW	Bit[5:0]: G41 of 8x8 G control point array for L/VS
0x5222	LENC_L_G42	0x00	RW	Bit[5:0]: G42 of 8x8 G control point array for L/VS
0x5223	LENC_L_G43	0x00	RW	Bit[5:0]: G43 of 8x8 G control point array for L/VS
0x5224	LENC_L_G44	0x00	RW	Bit[5:0]: G44 of 8x8 G control point array for L/VS
0x5225	LENC_L_G45	0x00	RW	Bit[5:0]: G45 of 8x8 G control point array for L/VS
0x5226	LENC_L_G46	0x00	RW	Bit[5:0]: G46 of 8x8 G control point array for L/VS
0x5227	LENC_L_G47	0x00	RW	Bit[5:0]: G47 of 8x8 G control point array for L/VS
0x5228	LENC_L_G50	0x00	RW	Bit[5:0]: G50 of 8x8 G control point array for L/VS
0x5229	LENC_L_G51	0x00	RW	Bit[5:0]: G51 of 8x8 G control point array for L/VS
0x522A	LENC_L_G52	0x00	RW	Bit[5:0]: G52 of 8x8 G control point array for L/VS
0x522B	LENC_L_G53	0x00	RW	Bit[5:0]: G53 of 8x8 G control point array for L/VS
0x522C	LENC_L_G54	0x00	RW	Bit[5:0]: G54 of 8x8 G control point array for L/VS
0x522D	LENC_L_G55	0x00	RW	Bit[5:0]: G55 of 8x8 G control point array for L/VS
0x522E	LENC_L_G56	0x00	RW	Bit[5:0]: G56 of 8x8 G control point array for L/VS
0x522F	LENC_L_G57	0x00	RW	Bit[5:0]: G57 of 8x8 G control point array for L/VS
0x5230	LENC_L_G60	0x00	RW	Bit[5:0]: G60 of 8x8 G control point array for L/VS
0x5231	LENC_L_G61	0x00	RW	Bit[5:0]: G61 of 8x8 G control point array for L/VS
0x5232	LENC_L_G62	0x00	RW	Bit[5:0]: G62 of 8x8 G control point array for L/VS
0x5233	LENC_L_G63	0x00	RW	Bit[5:0]: G63 of 8x8 G control point array for L/VS
0x5234	LENC_L_G64	0x00	RW	Bit[5:0]: G64 of 8x8 G control point array for L/VS
0x5235	LENC_L_G65	0x00	RW	Bit[5:0]: G65 of 8x8 G control point array for L/VS
0x5236	LENC_L_G66	0x00	RW	Bit[5:0]: G66 of 8x8 G control point array for L/VS
0x5237	LENC_L_G67	0x00	RW	Bit[5:0]: G67 of 8x8 G control point array for L/VS
0x5238	LENC_L_G70	0x00	RW	Bit[5:0]: G70 of 8x8 G control point array for L/VS
0x5239	LENC_L_G71	0x00	RW	Bit[5:0]: G71 of 8x8 G control point array for L/VS

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table 4-3 LENC control registers (sheet 4 of 18)

address	register name	default value	R/W	description
0x523A	LENC_L_G72	0x00	RW	Bit[5:0]: G72 of 8x8 G control point array for L/VS
0x523B	LENC_L_G73	0x00	RW	Bit[5:0]: G73 of 8x8 G control point array for L/VS
0x523C	LENC_L_G74	0x00	RW	Bit[5:0]: G74 of 8x8 G control point array for L/VS
0x523D	LENC_L_G75	0x00	RW	Bit[5:0]: G75 of 8x8 G control point array for L/VS
0x523E	LENC_L_G76	0x00	RW	Bit[5:0]: G76 of 8x8 G control point array for L/VS
0x523F	LENC_L_G77	0x00	RW	Bit[5:0]: G77 of 8x8 G control point array for L/VS
0x5240	LENC_L_B00	0x20	RW	Bit[5:0]: B00 of 8x8 B control point array for L/VS
0x5241	LENC_L_B01	0x20	RW	Bit[5:0]: B01 of 8x8 B control point array for L/VS
0x5242	LENC_L_B02	0x20	RW	Bit[5:0]: B02 of 8x8 B control point array for L/VS
0x5243	LENC_L_B03	0x20	RW	Bit[5:0]: B03 of 8x8 B control point array for L/VS
0x5244	LENC_L_B04	0x20	RW	Bit[5:0]: B04 of 8x8 B control point array for L/VS
0x5245	LENC_L_B05	0x20	RW	Bit[5:0]: B05 of 8x8 B control point array for L/VS
0x5246	LENC_L_B06	0x20	RW	Bit[5:0]: B06 of 8x8 B control point array for L/VS
0x5247	LENC_L_B07	0x20	RW	Bit[5:0]: B07 of 8x8 B control point array for L/VS
0x5248	LENC_L_B10	0x20	RW	Bit[5:0]: B10 of 8x8 B control point array for L/VS
0x5249	LENC_L_B11	0x20	RW	Bit[5:0]: B11 of 8x8 B control point array for L/VS
0x524A	LENC_L_B12	0x20	RW	Bit[5:0]: B12 of 8x8 B control point array for L/VS
0x524B	LENC_L_B13	0x20	RW	Bit[5:0]: B13 of 8x8 B control point array for L/VS
0x524C	LENC_L_B14	0x20	RW	Bit[5:0]: B14 of 8x8 B control point array for L/VS
0x524D	LENC_L_B15	0x20	RW	Bit[5:0]: B15 of 8x8 B control point array for L/VS
0x524E	LENC_L_B16	0x20	RW	Bit[5:0]: B16 of 8x8 B control point array for L/VS
0x524F	LENC_L_B17	0x20	RW	Bit[5:0]: B17 of 8x8 B control point array for L/VS
0x5250	LENC_L_B20	0x20	RW	Bit[5:0]: B20 of 8x8 B control point array for L/VS
0x5251	LENC_L_B21	0x20	RW	Bit[5:0]: B21 of 8x8 B control point array for L/VS
0x5252	LENC_L_B22	0x20	RW	Bit[5:0]: B22 of 8x8 B control point array for L/VS
0x5253	LENC_L_B23	0x20	RW	Bit[5:0]: B23 of 8x8 B control point array for L/VS
0x5254	LENC_L_B24	0x20	RW	Bit[5:0]: B24 of 8x8 B control point array for L/VS
0x5255	LENC_L_B25	0x20	RW	Bit[5:0]: B25 of 8x8 B control point array for L/VS

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table 4-3 LENC control registers (sheet 5 of 18)

address	register name	default value	R/W	description
0x5256	LENC_L_B26	0x20	RW	Bit[5:0]: B26 of 8x8 B control point array for L/VS
0x5257	LENC_L_B27	0x20	RW	Bit[5:0]: B27 of 8x8 B control point array for L/VS
0x5258	LENC_L_B30	0x20	RW	Bit[5:0]: B30 of 8x8 B control point array for L/VS
0x5259	LENC_L_B31	0x20	RW	Bit[5:0]: B31 of 8x8 B control point array for L/VS
0x525A	LENC_L_B32	0x20	RW	Bit[5:0]: B32 of 8x8 B control point array for L/VS
0x525B	LENC_L_B33	0x20	RW	Bit[5:0]: B33 of 8x8 B control point array for L/VS
0x525C	LENC_L_B34	0x20	RW	Bit[5:0]: B34 of 8x8 B control point array for L/VS
0x525D	LENC_L_B35	0x20	RW	Bit[5:0]: B35 of 8x8 B control point array for L/VS
0x525E	LENC_L_B36	0x20	RW	Bit[5:0]: B36 of 8x8 B control point array for L/VS
0x525F	LENC_L_B37	0x20	RW	Bit[5:0]: B37 of 8x8 B control point array for L/VS
0x5260	LENC_L_B40	0x20	RW	Bit[5:0]: B40 of 8x8 B control point array for L/VS
0x5261	LENC_L_B41	0x20	RW	Bit[5:0]: B41 of 8x8 B control point array for L/VS
0x5262	LENC_L_B42	0x20	RW	Bit[5:0]: B42 of 8x8 B control point array for L/VS
0x5263	LENC_L_B43	0x20	RW	Bit[5:0]: B43 of 8x8 B control point array for L/VS
0x5264	LENC_L_B44	0x20	RW	Bit[5:0]: B44 of 8x8 B control point array for L/VS
0x5265	LENC_L_B45	0x20	RW	Bit[5:0]: B45 of 8x8 B control point array for L/VS
0x5266	LENC_L_B46	0x20	RW	Bit[5:0]: B46 of 8x8 B control point array for L/VS
0x5267	LENC_L_B47	0x20	RW	Bit[5:0]: B47 of 8x8 B control point array for L/VS
0x5268	LENC_L_B50	0x20	RW	Bit[5:0]: B50 of 8x8 B control point array for L/VS
0x5269	LENC_L_B51	0x20	RW	Bit[5:0]: B51 of 8x8 B control point array for L/VS
0x526A	LENC_L_B52	0x20	RW	Bit[5:0]: B52 of 8x8 B control point array for L/VS
0x526B	LENC_L_B53	0x20	RW	Bit[5:0]: B53 of 8x8 B control point array for L/VS
0x526C	LENC_L_B54	0x20	RW	Bit[5:0]: B54 of 8x8 B control point array for L/VS
0x526D	LENC_L_B55	0x20	RW	Bit[5:0]: B55 of 8x8 B control point array for L/VS
0x526E	LENC_L_B56	0x20	RW	Bit[5:0]: B56 of 8x8 B control point array for L/VS
0x526F	LENC_L_B57	0x20	RW	Bit[5:0]: B57 of 8x8 B control point array for L/VS
0x5270	LENC_L_B60	0x20	RW	Bit[5:0]: B60 of 8x8 B control point array for L/VS
0x5271	LENC_L_B61	0x20	RW	Bit[5:0]: B61 of 8x8 B control point array for L/VS

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table 4-3 LENC control registers (sheet 6 of 18)

address	register name	default value	R/W	description
0x5272	LENC_L_B62	0x20	RW	Bit[5:0]: B62 of 8x8 B control point array for L/VS
0x5273	LENC_L_B63	0x20	RW	Bit[5:0]: B63 of 8x8 B control point array for L/VS
0x5274	LENC_L_B64	0x20	RW	Bit[5:0]: B64 of 8x8 B control point array for L/VS
0x5275	LENC_L_B65	0x20	RW	Bit[5:0]: B65 of 8x8 B control point array for L/VS
0x5276	LENC_L_B66	0x20	RW	Bit[5:0]: B66 of 8x8 B control point array for L/VS
0x5277	LENC_L_B67	0x20	RW	Bit[5:0]: B67 of 8x8 B control point array for L/VS
0x5278	LENC_L_B70	0x20	RW	Bit[5:0]: B70 of 8x8 B control point array for L/VS
0x5279	LENC_L_B71	0x20	RW	Bit[5:0]: B71 of 8x8 B control point array for L/VS
0x527A	LENC_L_B72	0x20	RW	Bit[5:0]: B72 of 8x8 B control point array for L/VS
0x527B	LENC_L_B73	0x20	RW	Bit[5:0]: B73 of 8x8 B control point array for L/VS
0x527C	LENC_L_B74	0x20	RW	Bit[5:0]: B74 of 8x8 B control point array for L/VS
0x527D	LENC_L_B75	0x20	RW	Bit[5:0]: B75 of 8x8 B control point array for L/VS
0x527E	LENC_L_B76	0x20	RW	Bit[5:0]: B76 of 8x8 B control point array for L/VS
0x527F	LENC_L_B77	0x20	RW	Bit[5:0]: B77 of 8x8 B control point array for L/VS
0x5280	LENC_L_R00	0x20	RW	Bit[5:0]: R00 of 8x8 R control point array for L/VS
0x5281	LENC_L_R01	0x20	RW	Bit[5:0]: R01 of 8x8 R control point array for L/VS
0x5282	LENC_L_R02	0x20	RW	Bit[5:0]: R02 of 8x8 R control point array for L/VS
0x5283	LENC_L_R03	0x20	RW	Bit[5:0]: R03 of 8x8 R control point array for L/VS
0x5284	LENC_L_R04	0x20	RW	Bit[5:0]: R04 of 8x8 R control point array for L/VS
0x5285	LENC_L_R05	0x20	RW	Bit[5:0]: R05 of 8x8 R control point array for L/VS
0x5286	LENC_L_R06	0x20	RW	Bit[5:0]: R06 of 8x8 R control point array for L/VS
0x5287	LENC_L_R07	0x20	RW	Bit[5:0]: R07 of 8x8 R control point array for L/VS
0x5288	LENC_L_R10	0x20	RW	Bit[5:0]: R10 of 8x8 R control point array for L/VS
0x5289	LENC_L_R11	0x20	RW	Bit[5:0]: R11 of 8x8 R control point array for L/VS
0x528A	LENC_L_R12	0x20	RW	Bit[5:0]: R12 of 8x8 R control point array for L/VS
0x528B	LENC_L_R13	0x20	RW	Bit[5:0]: R13 of 8x8 R control point array for L/VS
0x528C	LENC_L_R14	0x20	RW	Bit[5:0]: R14 of 8x8 R control point array for L/VS
0x528D	LENC_L_R15	0x20	RW	Bit[5:0]: R15 of 8x8 R control point array for L/VS

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table 4-3 LENC control registers (sheet 7 of 18)

address	register name	default value	R/W	description
0x528E	LENC_L_R16	0x20	RW	Bit[5:0]: R16 of 8x8 R control point array for L/VS
0x528F	LENC_L_R17	0x20	RW	Bit[5:0]: R17 of 8x8 R control point array for L/VS
0x5290	LENC_L_R20	0x20	RW	Bit[5:0]: R20 of 8x8 R control point array for L/VS
0x5291	LENC_L_R21	0x20	RW	Bit[5:0]: R21 of 8x8 R control point array for L/VS
0x5292	LENC_L_R22	0x20	RW	Bit[5:0]: R22 of 8x8 R control point array for L/VS
0x5293	LENC_L_R23	0x20	RW	Bit[5:0]: R23 of 8x8 R control point array for L/VS
0x5294	LENC_L_R24	0x20	RW	Bit[5:0]: R24 of 8x8 R control point array for L/VS
0x5295	LENC_L_R25	0x20	RW	Bit[5:0]: R25 of 8x8 R control point array for L/VS
0x5296	LENC_L_R26	0x20	RW	Bit[5:0]: R26 of 8x8 R control point array for L/VS
0x5297	LENC_L_R27	0x20	RW	Bit[5:0]: R27 of 8x8 R control point array for L/VS
0x5298	LENC_L_R30	0x20	RW	Bit[5:0]: R30 of 8x8 R control point array for L/VS
0x5299	LENC_L_R31	0x20	RW	Bit[5:0]: R31 of 8x8 R control point array for L/VS
0x529A	LENC_L_R32	0x20	RW	Bit[5:0]: R32 of 8x8 R control point array for L/VS
0x529B	LENC_L_R33	0x20	RW	Bit[5:0]: R33 of 8x8 R control point array for L/VS
0x529C	LENC_L_R34	0x20	RW	Bit[5:0]: R34 of 8x8 R control point array for L/VS
0x529D	LENC_L_R35	0x20	RW	Bit[5:0]: R35 of 8x8 R control point array for L/VS
0x529E	LENC_L_R36	0x20	RW	Bit[5:0]: R36 of 8x8 R control point array for L/VS
0x529F	LENC_L_R37	0x20	RW	Bit[5:0]: R37 of 8x8 R control point array for L/VS
0x52A0	LENC_L_R40	0x20	RW	Bit[5:0]: R40 of 8x8 R control point array for L/VS
0x52A1	LENC_L_R41	0x20	RW	Bit[5:0]: R41 of 8x8 R control point array for L/VS
0x52A2	LENC_L_R42	0x20	RW	Bit[5:0]: R42 of 8x8 R control point array for L/VS
0x52A3	LENC_L_R43	0x20	RW	Bit[5:0]: R43 of 8x8 R control point array for L/VS
0x52A4	LENC_L_R44	0x20	RW	Bit[5:0]: R44 of 8x8 R control point array for L/VS
0x52A5	LENC_L_R45	0x20	RW	Bit[5:0]: R45 of 8x8 R control point array for L/VS
0x52A6	LENC_L_R46	0x20	RW	Bit[5:0]: R46 of 8x8 R control point array for L/VS
0x52A7	LENC_L_R47	0x20	RW	Bit[5:0]: R47 of 8x8 R control point array for L/VS
0x52A8	LENC_L_R50	0x20	RW	Bit[5:0]: R50 of 8x8 R control point array for L/VS
0x52A9	LENC_L_R51	0x20	RW	Bit[5:0]: R51 of 8x8 R control point array for L/VS

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table 4-3 LENC control registers (sheet 8 of 18)

address	register name	default value	R/W	description
0x52AA	LENC_L_R52	0x20	RW	Bit[5:0]: R52 of 8x8 R control point array for L/VS
0x52AB	LENC_L_R53	0x20	RW	Bit[5:0]: R53 of 8x8 R control point array for L/VS
0x52AC	LENC_L_R54	0x20	RW	Bit[5:0]: R54 of 8x8 R control point array for L/VS
0x52AD	LENC_L_R55	0x20	RW	Bit[5:0]: R55 of 8x8 R control point array for L/VS
0x52AE	LENC_L_R56	0x20	RW	Bit[5:0]: R56 of 8x8 R control point array for L/VS
0x52AF	LENC_L_R57	0x20	RW	Bit[5:0]: R57 of 8x8 R control point array for L/VS
0x52B0	LENC_L_R60	0x20	RW	Bit[5:0]: R60 of 8x8 R control point array for L/VS
0x52B1	LENC_L_R61	0x20	RW	Bit[5:0]: R61 of 8x8 R control point array for L/VS
0x52B2	LENC_L_R62	0x20	RW	Bit[5:0]: R62 of 8x8 R control point array for L/VS
0x52B3	LENC_L_R63	0x20	RW	Bit[5:0]: R63 of 8x8 R control point array for L/VS
0x52B4	LENC_L_R64	0x20	RW	Bit[5:0]: R64 of 8x8 R control point array for L/VS
0x52B5	LENC_L_R65	0x20	RW	Bit[5:0]: R65 of 8x8 R control point array for L/VS
0x52B6	LENC_L_R66	0x20	RW	Bit[5:0]: R66 of 8x8 R control point array for L/VS
0x52B7	LENC_L_R67	0x20	RW	Bit[5:0]: R67 of 8x8 R control point array for L/VS
0x52B8	LENC_L_R70	0x20	RW	Bit[5:0]: R70 of 8x8 R control point array for L/VS
0x52B9	LENC_L_R71	0x20	RW	Bit[5:0]: R71 of 8x8 R control point array for L/VS
0x52BA	LENC_L_R72	0x20	RW	Bit[5:0]: R72 of 8x8 R control point array for L/VS
0x52BB	LENC_L_R73	0x20	RW	Bit[5:0]: R73 of 8x8 R control point array for L/VS
0x52BC	LENC_L_R74	0x20	RW	Bit[5:0]: R74 of 8x8 R control point array for L/VS
0x52BD	LENC_L_R75	0x20	RW	Bit[5:0]: R75 of 8x8 R control point array for L/VS
0x52BE	LENC_L_R76	0x20	RW	Bit[5:0]: R76 of 8x8 R control point array for L/VS
0x52BF	LENC_L_R77	0x20	RW	Bit[5:0]: R77 of 8x8 R control point array for L/VS
0x52C0	LENC_S_G00	0x00	RW	Bit[5:0]: G00 of 8x8 G control point array for S
0x52C1	LENC_S_G01	0x00	RW	Bit[5:0]: G01 of 8x8 G control point array for S
0x52C2	LENC_S_G02	0x00	RW	Bit[5:0]: G02 of 8x8 G control point array for S
0x52C3	LENC_S_G03	0x00	RW	Bit[5:0]: G03 of 8x8 G control point array for S
0x52C4	LENC_S_G04	0x00	RW	Bit[5:0]: G04 of 8x8 G control point array for S
0x52C5	LENC_S_G05	0x00	RW	Bit[5:0]: G05 of 8x8 G control point array for S

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table 4-3 LENC control registers (sheet 9 of 18)

address	register name	default value	R/W	description
0x52C6	LENC_S_G06	0x00	RW	Bit[5:0]: G06 of 8x8 G control point array for S
0x52C7	LENC_S_G07	0x00	RW	Bit[5:0]: G07 of 8x8 G control point array for S
0x52C8	LENC_S_G10	0x00	RW	Bit[5:0]: G10 of 8x8 G control point array for S
0x52C9	LENC_S_G11	0x00	RW	Bit[5:0]: G11 of 8x8 G control point array for S
0x52CA	LENC_S_G12	0x00	RW	Bit[5:0]: G12 of 8x8 G control point array for S
0x52CB	LENC_S_G13	0x00	RW	Bit[5:0]: G13 of 8x8 G control point array for S
0x52CC	LENC_S_G14	0x00	RW	Bit[5:0]: G14 of 8x8 G control point array for S
0x52CD	LENC_S_G15	0x00	RW	Bit[5:0]: G15 of 8x8 G control point array for S
0x52CE	LENC_S_G16	0x00	RW	Bit[5:0]: G16 of 8x8 G control point array for S
0x52CF	LENC_S_G17	0x00	RW	Bit[5:0]: G17 of 8x8 G control point array for S
0x52D0	LENC_S_G20	0x00	RW	Bit[5:0]: G20 of 8x8 G control point array for S
0x52D1	LENC_S_G21	0x00	RW	Bit[5:0]: G21 of 8x8 G control point array for S
0x52D2	LENC_S_G22	0x00	RW	Bit[5:0]: G22 of 8x8 G control point array for S
0x52D3	LENC_S_G23	0x00	RW	Bit[5:0]: G23 of 8x8 G control point array for S
0x52D4	LENC_S_G24	0x00	RW	Bit[5:0]: G24 of 8x8 G control point array for S
0x52D5	LENC_S_G25	0x00	RW	Bit[5:0]: G25 of 8x8 G control point array for S
0x52D6	LENC_S_G26	0x00	RW	Bit[5:0]: G26 of 8x8 G control point array for S
0x52D7	LENC_S_G27	0x00	RW	Bit[5:0]: G27 of 8x8 G control point array for S
0x52D8	LENC_S_G30	0x00	RW	Bit[5:0]: G30 of 8x8 G control point array for S
0x52D9	LENC_S_G31	0x00	RW	Bit[5:0]: G31 of 8x8 G control point array for S
0x52DA	LENC_S_G32	0x00	RW	Bit[5:0]: G32 of 8x8 G control point array for S
0x52DB	LENC_S_G33	0x00	RW	Bit[5:0]: G33 of 8x8 G control point array for S
0x52DC	LENC_S_G34	0x00	RW	Bit[5:0]: G34 of 8x8 G control point array for S
0x52DD	LENC_S_G35	0x00	RW	Bit[5:0]: G35 of 8x8 G control point array for S
0x52DE	LENC_S_G36	0x00	RW	Bit[5:0]: G36 of 8x8 G control point array for S
0x52DF	LENC_S_G37	0x00	RW	Bit[5:0]: G37 of 8x8 G control point array for S
0x52E0	LENC_S_G40	0x00	RW	Bit[5:0]: G40 of 8x8 G control point array for S
0x52E1	LENC_S_G41	0x00	RW	Bit[5:0]: G41 of 8x8 G control point array for S

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table 4-3 LENC control registers (sheet 10 of 18)

address	register name	default value	R/W	description
0x52E2	LENC_S_G42	0x00	RW	Bit[5:0]: G42 of 8x8 G control point array for S
0x52E3	LENC_S_G43	0x00	RW	Bit[5:0]: G43 of 8x8 G control point array for S
0x52E4	LENC_S_G44	0x00	RW	Bit[5:0]: G44 of 8x8 G control point array for S
0x52E5	LENC_S_G45	0x00	RW	Bit[5:0]: G45 of 8x8 G control point array for S
0x52E6	LENC_S_G46	0x00	RW	Bit[5:0]: G46 of 8x8 G control point array for S
0x52E7	LENC_S_G47	0x00	RW	Bit[5:0]: G47 of 8x8 G control point array for S
0x52E8	LENC_S_G50	0x00	RW	Bit[5:0]: G50 of 8x8 G control point array for S
0x52E9	LENC_S_G51	0x00	RW	Bit[5:0]: G51 of 8x8 G control point array for S
0x52EA	LENC_S_G52	0x00	RW	Bit[5:0]: G52 of 8x8 G control point array for S
0x52EB	LENC_S_G53	0x00	RW	Bit[5:0]: G53 of 8x8 G control point array for S
0x52EC	LENC_S_G54	0x00	RW	Bit[5:0]: G54 of 8x8 G control point array for S
0x52ED	LENC_S_G55	0x00	RW	Bit[5:0]: G55 of 8x8 G control point array for S
0x52EE	LENC_S_G56	0x00	RW	Bit[5:0]: G56 of 8x8 G control point array for S
0x52EF	LENC_S_G57	0x00	RW	Bit[5:0]: G57 of 8x8 G control point array for S
0x52F0	LENC_S_G60	0x00	RW	Bit[5:0]: G60 of 8x8 G control point array for S
0x52F1	LENC_S_G61	0x00	RW	Bit[5:0]: G61 of 8x8 G control point array for S
0x52F2	LENC_S_G62	0x00	RW	Bit[5:0]: G62 of 8x8 G control point array for S
0x52F3	LENC_S_G63	0x00	RW	Bit[5:0]: G63 of 8x8 G control point array for S
0x52F4	LENC_S_G64	0x00	RW	Bit[5:0]: G64 of 8x8 G control point array for S
0x52F5	LENC_S_G65	0x00	RW	Bit[5:0]: G65 of 8x8 G control point array for S
0x52F6	LENC_S_G66	0x00	RW	Bit[5:0]: G66 of 8x8 G control point array for S
0x52F7	LENC_S_G67	0x00	RW	Bit[5:0]: G67 of 8x8 G control point array for S
0x52F8	LENC_S_G70	0x00	RW	Bit[5:0]: G70 of 8x8 G control point array for S
0x52F9	LENC_S_G71	0x00	RW	Bit[5:0]: G71 of 8x8 G control point array for S
0x52FA	LENC_S_G72	0x00	RW	Bit[5:0]: G72 of 8x8 G control point array for S
0x52FB	LENC_S_G73	0x00	RW	Bit[5:0]: G73 of 8x8 G control point array for S
0x52FC	LENC_S_G74	0x00	RW	Bit[5:0]: G74 of 8x8 G control point array for S
0x52FD	LENC_S_G75	0x00	RW	Bit[5:0]: G75 of 8x8 G control point array for S

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table 4-3 LENC control registers (sheet 11 of 18)

address	register name	default value	R/W	description
0x52FE	LENC_S_G76	0x00	RW	Bit[5:0]: G76 of 8x8 G control point array for S
0x52FF	LENC_S_G77	0x00	RW	Bit[5:0]: G77 of 8x8 G control point array for S
0x5300	LENC_S_B00	0x20	RW	Bit[5:0]: B00 of 8x8 B control point array for S
0x5301	LENC_S_B01	0x20	RW	Bit[5:0]: B01 of 8x8 B control point array for S
0x5302	LENC_S_B02	0x20	RW	Bit[5:0]: B02 of 8x8 B control point array for S
0x5303	LENC_S_B03	0x20	RW	Bit[5:0]: B03 of 8x8 B control point array for S
0x5304	LENC_S_B04	0x20	RW	Bit[5:0]: B04 of 8x8 B control point array for S
0x5305	LENC_S_B05	0x20	RW	Bit[5:0]: B05 of 8x8 B control point array for S
0x5306	LENC_S_B06	0x20	RW	Bit[5:0]: B06 of 8x8 B control point array for S
0x5307	LENC_S_B07	0x20	RW	Bit[5:0]: B07 of 8x8 B control point array for S
0x5308	LENC_S_B10	0x20	RW	Bti[5:0]: B10 of 8x8 B control point array for S
0x5309	LENC_S_B11	0x20	RW	Bit[5:0]: B11 of 8x8 B control point array for S
0x530A	LENC_S_B12	0x20	RW	Bit[5:0]: B12 of 8x8 B control point array for S
0x530B	LENC_S_B13	0x20	RW	Bit[5:0]: B13 of 8x8 B control point array for S
0x530C	LENC_S_B14	0x20	RW	Bit[5:0]: B14 of 8x8 B control point array for S
0x530D	LENC_S_B15	0x20	RW	Bit[5:0]: B15 of 8x8 B control point array for S
0x530E	LENC_S_B16	0x20	RW	Bit[5:0]: B16 of 8x8 B control point array for S
0x530F	LENC_S_B17	0x20	RW	Bit[5:0]: B17 of 8x8 B control point array for S
0x5310	LENC_S_B20	0x20	RW	Bit[5:0]: B20 of 8x8 B control point array for S
0x5311	LENC_S_B21	0x20	RW	Bit[5:0]: B21 of 8x8 B control point array for S
0x5312	LENC_S_B22	0x20	RW	Bit[5:0]: B22 of 8x8 B control point array for S
0x5313	LENC_S_B23	0x20	RW	Bit[5:0]: B23 of 8x8 B control point array for S
0x5314	LENC_S_B24	0x20	RW	Bit[5:0]: B24 of 8x8 B control point array for S
0x5315	LENC_S_B25	0x20	RW	Bit[5:0]: B25 of 8x8 B control point array for S
0x5316	LENC_S_B26	0x20	RW	Bit[5:0]: B26 of 8x8 B control point array for S
0x5317	LENC_S_B27	0x20	RW	Bit[5:0]: B27 of 8x8 B control point array for S
0x5318	LENC_S_B30	0x20	RW	Bit[5:0]: B30 of 8x8 B control point array for S
0x5319	LENC_S_B31	0x20	RW	Bit[5:0]: B31 of 8x8 B control point array for S

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table 4-3 LENC control registers (sheet 12 of 18)

address	register name	default value	R/W	description
0x531A	LENC_S_B32	0x20	RW	Bit[5:0]: B32 of 8x8 B control point array for S
0x531B	LENC_S_B33	0x20	RW	Bit[5:0]: B33 of 8x8 B control point array for S
0x531C	LENC_S_B34	0x20	RW	Bit[5:0]: B34 of 8x8 B control point array for S
0x531D	LENC_S_B35	0x20	RW	Bit[5:0]: B35 of 8x8 B control point array for S
0x531E	LENC_S_B36	0x20	RW	Bit[5:0]: B36 of 8x8 B control point array for S
0x531F	LENC_S_B37	0x20	RW	Bit[5:0]: B37 of 8x8 B control point array for S
0x5320	LENC_S_B40	0x20	RW	Bit[5:0]: B40 of 8x8 B control point array for S
0x5321	LENC_S_B41	0x20	RW	Bit[5:0]: B41 of 8x8 B control point array for S
0x5322	LENC_S_B42	0x20	RW	Bit[5:0]: B42 of 8x8 B control point array for S
0x5323	LENC_S_B43	0x20	RW	Bit[5:0]: B43 of 8x8 B control point array for S
0x5324	LENC_S_B44	0x20	RW	Bit[5:0]: B44 of 8x8 B control point array for S
0x5325	LENC_S_B45	0x20	RW	Bit[5:0]: B45 of 8x8 B control point array for S
0x5326	LENC_S_B46	0x20	RW	Bit[5:0]: B46 of 8x8 B control point array for S
0x5327	LENC_S_B47	0x20	RW	Bit[5:0]: B47 of 8x8 B control point array for S
0x5328	LENC_S_B50	0x20	RW	Bit[5:0]: B50 of 8x8 B control point array for S
0x5329	LENC_S_B51	0x20	RW	Bit[5:0]: B51 of 8x8 B control point array for S
0x532A	LENC_S_B52	0x20	RW	Bit[5:0]: B52 of 8x8 B control point array for S
0x532B	LENC_S_B53	0x20	RW	Bit[5:0]: B53 of 8x8 B control point array for S
0x532C	LENC_S_B54	0x20	RW	Bit[5:0]: B54 of 8x8 B control point array for S
0x532D	LENC_S_B55	0x20	RW	Bit[5:0]: B55 of 8x8 B control point array for S
0x532E	LENC_S_B56	0x20	RW	Bit[5:0]: B56 of 8x8 B control point array for S
0x532F	LENC_S_B57	0x20	RW	Bit[5:0]: B57 of 8x8 B control point array for S
0x5330	LENC_S_B60	0x20	RW	Bit[5:0]: B60 of 8x8 B control point array for S
0x5331	LENC_S_B61	0x20	RW	Bit[5:0]: B61 of 8x8 B control point array for S
0x5332	LENC_S_B62	0x20	RW	Bit[5:0]: B62 of 8x8 B control point array for S
0x5333	LENC_S_B63	0x20	RW	Bit[5:0]: B63 of 8x8 B control point array for S
0x5334	LENC_S_B64	0x20	RW	Bit[5:0]: B64 of 8x8 B control point array for S
0x5335	LENC_S_B65	0x20	RW	Bit[5:0]: B65 of 8x8 B control point array for S

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table 4-3 LENC control registers (sheet 13 of 18)

address	register name	default value	R/W	description
0x5336	LENC_S_B66	0x20	RW	Bit[5:0]: B66 of 8x8 B control point array for S
0x5337	LENC_S_B67	0x20	RW	Bit[5:0]: B67 of 8x8 B control point array for S
0x5338	LENC_S_B70	0x20	RW	Bit[5:0]: B70 of 8x8 B control point array for S
0x5339	LENC_S_B71	0x20	RW	Bit[5:0]: B71 of 8x8 B control point array for S
0x533A	LENC_S_B72	0x20	RW	Bit[5:0]: B72 of 8x8 B control point array for S
0x533B	LENC_S_B73	0x20	RW	Bit[5:0]: B73 of 8x8 B control point array for S
0x533C	LENC_S_B74	0x20	RW	Bit[5:0]: B74 of 8x8 B control point array for S
0x533D	LENC_S_B75	0x20	RW	Bit[5:0]: B75 of 8x8 B control point array for S
0x533E	LENC_S_B76	0x20	RW	Bit[5:0]: B76 of 8x8 B control point array for S
0x533F	LENC_S_B77	0x20	RW	Bit[5:0]: B77 of 8x8 B control point array for S
0x5340	LENC_S_R00	0x20	RW	Bit[5:0]: R00 of 8x8 R control point array for S
0x5341	LENC_S_R01	0x20	RW	Bit[5:0]: R01 of 8x8 R control point array for S
0x5342	LENC_S_R02	0x20	RW	Bit[5:0]: R02 of 8x8 R control point array for S
0x5343	LENC_S_R03	0x20	RW	Bit[5:0]: R03 of 8x8 R control point array for S
0x5344	LENC_S_R04	0x20	RW	Bit[5:0]: R04 of 8x8 R control point array for S
0x5345	LENC_S_R05	0x20	RW	Bit[5:0]: R05 of 8x8 R control point array for S
0x5346	LENC_S_R06	0x20	RW	Bit[5:0]: R06 of 8x8 R control point array for S
0x5347	LENC_S_R07	0x20	RW	Bit[5:0]: R07 of 8x8 R control point array for S
0x5348	LENC_S_R10	0x20	RW	Bit[5:0]: R10 of 8x8 R control point array for S
0x5349	LENC_S_R11	0x20	RW	Bit[5:0]: R11 of 8x8 R control point array for S
0x534A	LENC_S_R12	0x20	RW	Bit[5:0]: R12 of 8x8 R control point array for S
0x534B	LENC_S_R13	0x20	RW	Bit[5:0]: R13 of 8x8 R control point array for S
0x534C	LENC_S_R14	0x20	RW	Bit[5:0]: R14 of 8x8 R control point array for S
0x534D	LENC_S_R15	0x20	RW	Bit[5:0]: R15 of 8x8 R control point array for S
0x534E	LENC_S_R16	0x20	RW	Bit[5:0]: R16 of 8x8 R control point array for S
0x534F	LENC_S_R17	0x20	RW	Bit[5:0]: R17 of 8x8 R control point array for S
0x5350	LENC_S_R20	0x20	RW	Bit[5:0]: R20 of 8x8 R control point array for S
0x5351	LENC_S_R21	0x20	RW	Bit[5:0]: R21 of 8x8 R control point array for S

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table 4-3 LENC control registers (sheet 14 of 18)

address	register name	default value	R/W	description
0x5352	LENC_S_R22	0x20	RW	Bit[5:0]: R22 of 8x8 R control point array for S
0x5353	LENC_S_R23	0x20	RW	Bit[5:0]: R23 of 8x8 R control point array for S
0x5354	LENC_S_R24	0x20	RW	Bit[5:0]: R24 of 8x8 R control point array for S
0x5355	LENC_S_R25	0x20	RW	Bit[5:0]: R25 of 8x8 R control point array for S
0x5356	LENC_S_R26	0x20	RW	Bit[5:0]: R26 of 8x8 R control point array for S
0x5357	LENC_S_R27	0x20	RW	Bit[5:0]: R27 of 8x8 R control point array for S
0x5358	LENC_S_R30	0x20	RW	Bit[5:0]: R30 of 8x8 R control point array for S
0x5359	LENC_S_R31	0x20	RW	Bit[5:0]: R31 of 8x8 R control point array for S
0x535A	LENC_S_R32	0x20	RW	Bit[5:0]: R32 of 8x8 R control point array for S
0x535B	LENC_S_R33	0x20	RW	Bit[5:0]: R33 of 8x8 R control point array for S
0x535C	LENC_S_R34	0x20	RW	Bit[5:0]: R34 of 8x8 R control point array for S
0x535D	LENC_S_R35	0x20	RW	Bit[5:0]: R35 of 8x8 R control point array for S
0x535E	LENC_S_R36	0x20	RW	Bit[5:0]: R36 of 8x8 R control point array for S
0x535F	LENC_S_R37	0x20	RW	Bit[5:0]: R37 of 8x8 R control point array for S
0x5360	LENC_S_R40	0x20	RW	Bit[5:0]: R40 of 8x8 R control point array for S
0x5361	LENC_S_R41	0x20	RW	Bit[5:0]: R41 of 8x8 R control point array for S
0x5362	LENC_S_R42	0x20	RW	Bit[5:0]: R42 of 8x8 R control point array for S
0x5363	LENC_S_R43	0x20	RW	Bit[5:0]: R43 of 8x8 R control point array for S
0x5364	LENC_S_R44	0x20	RW	Bit[5:0]: R44 of 8x8 R control point array for S
0x5365	LENC_S_R45	0x20	RW	Bit[5:0]: R45 of 8x8 R control point array for S
0x5366	LENC_S_R46	0x20	RW	Bit[5:0]: R46 of 8x8 R control point array for S
0x5367	LENC_S_R47	0x20	RW	Bit[5:0]: R47 of 8x8 R control point array for S
0x5368	LENC_S_R50	0x20	RW	Bit[5:0]: R50 of 8x8 R control point array for S
0x5369	LENC_S_R51	0x20	RW	Bit[5:0]: R51 of 8x8 R control point array for S
0x536A	LENC_S_R52	0x20	RW	Bit[5:0]: R52 of 8x8 R control point array for S
0x536B	LENC_S_R53	0x20	RW	Bit[5:0]: R53 of 8x8 R control point array for S
0x536C	LENC_S_R54	0x20	RW	Bit[5:0]: R54 of 8x8 R control point array for S
0x536D	LENC_S_R55	0x20	RW	Bit[5:0]: R55 of 8x8 R control point array for S

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table 4-3 LENC control registers (sheet 15 of 18)

address	register name	default value	R/W	description
0x536E	LENC_S_R56	0x20	RW	Bit[5:0]: R56 of 8x8 R control point array for S
0x536F	LENC_S_R57	0x20	RW	Bit[5:0]: R57 of 8x8 R control point array for S
0x5370	LENC_S_R60	0x20	RW	Bit[5:0]: R60 of 8x8 R control point array for S
0x5371	LENC_S_R61	0x20	RW	Bit[5:0]: R61 of 8x8 R control point array for S
0x5372	LENC_S_R62	0x20	RW	Bit[5:0]: R62 of 8x8 R control point array for S
0x5373	LENC_S_R63	0x20	RW	Bit[5:0]: R63 of 8x8 R control point array for S
0x5374	LENC_S_R64	0x20	RW	Bit[5:0]: R64 of 8x8 R control point array for S
0x5375	LENC_S_R65	0x20	RW	Bit[5:0]: R65 of 8x8 R control point array for S
0x5376	LENC_S_R66	0x20	RW	Bit[5:0]: R66 of 8x8 R control point array for S
0x5377	LENC_S_R67	0x20	RW	Bit[5:0]: R67 of 8x8 R control point array for S
0x5378	LENC_S_R70	0x20	RW	Bit[5:0]: R70 of 8x8 R control point array for S
0x5379	LENC_S_R71	0x20	RW	Bit[5:0] R71 of 8x8 R control point array for S
0x537A	LENC_S_R72	0x20	RW	Bit[5:0]: R72 of 8x8 R control point array for S
0x537B	LENC_S_R73	0x20	RW	Bit[5:0]: R73 of 8x8 R control point array for S
0x537C	LENC_S_R74	0x20	RW	Bit[5:0]: R74 of 8x8 R control point array for S
0x537D	LENC_S_R75	0x20	RW	Bit[5:0]: R75 of 8x8 R control point array for S
0x537E	LENC_S_R76	0x20	RW	Bit[5:0]: R76 of 8x8 R control point array for S
0x537F	LENC_S_R77	0x20	RW	Bit[5:0]: R77 of 8x8 R control point array for S
0x5380	LENC_CTRL10	0x0D	RW	Bit[3]: m_nq_option L/S/VS employ same m_nq of L Bit[2]: Gain 0: Do not allow less than 1x gain 1: Allow less than 1x gain to apply to pixel Bit[1]: rand_bit_en_l (active high) Add random enable for L/VS Bit[0]: Luminance 0: Luminance compensation amplitude does not change with sensor gain 1: Luminance compensation amplitude changes with camera gain

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table 4-3 LENC control registers (sheet 16 of 18)

address	register name	default value	R/W	description
0x5381	MAXGAIN_L_BYTE1	0x00	RW	Bit[3:0]: Maxgain[11:8] If 0x5380[0]=1 and sensor gain is bigger than this threshold, luminance compensation amplitude will be the minimum value (0x5385)
0x5382	MAXGAIN_L_BYTE0	0x60	RW	Bit[7:0]: Maxgain[7:0] If 0x5380[0]=1 and sensor gain is bigger than this threshold, luminance compensation amplitude will be the minimum value (0x5385)
0x5383	MINGAIN_L_BYTE1	0x00	RW	Bit[3:0]: Mingain[11:8] If 0x5380[0]=1 and sensor gain is smaller than this threshold, luminance compensation amplitude will be the maximum value (0x5386)
0x5384	MINGAIN_L_BYTE0	0x20	RW	Bit[7:0]: Mingain[7:0] If 0x5380[0]=1 and sensor gain is smaller than this threshold, luminance compensation amplitude will be the maximum value (0x5386)
0x5385	MINQ_L	0x18	RW	Bit[6:0]: Value indicates minimum amplitude which luminance channel compensates when 0x5380[0]=1
0x5386	MAXQ_L	0x40	RW	Bit[6:0]: Value indicates maximum amplitude which luminance channel compensates when 0x5380[0]=1
0x5387	BR_HSCALE_L_ BYTE1	0x02	RW	Bit[2:0]: BR_HSCALE[10:8] For horizontal color gain calculation, this value indicates step between two connected horizontal pixels
0x5388	BR_HSCALE_L_ BYTE0	0x0A	RW	Bit[7:0]: BR_HSCALE[7:0] For horizontal color gain calculation, this value indicates step between two connected horizontal pixels
0x5389	BR_VSCALE_L_ BYTE1	0x02	RW	Bit[2:0]: BR_VSCALE[10:8] For vertical color gain calculation, value indicates step between two connected vertical pixels
0x538A	BR_VSCALE_L_ BYTE0	0xF4	RW	Bit[7:0]: BR_VSCALE[7:0] For vertical color gain calculation, value indicates step between two connected vertical pixels

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table 4-3 LENC control registers (sheet 17 of 18)

address	register name	default value	R/W	description
0x538B	G_HSCALE_L_ BYTE1	0x02	RW	Bit[2:0]: G_HSCALE[10:8] For horizontal luminance gain calculation, this value indicates step between two connected horizontal pixels
0x538C	G_HSCALE_L_ BYTE0	0x06	RW	Bit[7:0]: G_HSCALE[7:0] For horizontal luminance gain calculation, this value indicates step between two connected horizontal pixels
0x538D	G_VSCALE_L_ BYTE1	0x01	RW	Bit[2:0]: G_VSCALE[10:8] For vertical luminance gain calculation, value indicates step between two connection vertical pixels
0x538E	G_VSCALE_L_ BYTE0	0x6A	RW	Bit[7:0]: G_VSCALE[7:0] For vertical luminance gain calculation, value indicates step between two connection vertical pixels
0x538F	LENC_CTRL11	0x6A	RW	Bit[2]: less_1x_en_s (active high) Less than 1x gain enable for S Bit[1]: rand_bit_en_s (active high) Add random enable for S Bit[0]: auto_q_en_s (active high) Auto calculation Q enable for S
0x5390	MAXGAIN_S_BYTE1	0x00	RW	Bit[3:0]: Upper gain threshold for auto Q, for S[11:8]
0x5391	MAXGAIN_S_BYTE0	0x60	RW	Bit[7:0]: Upper gain threshold for auto Q, for S[7:0]
0x5392	MINGAIN_S_BYTE1	0x00	RW	Bit[3:0]: Lower gain threshold for auto Q, for S[11:8]
0x5393	MINGAIN_S_BYTE0	0x20	RW	Bit[7:0]: Lower gain threshold for auto Q, for S[7:0]
0x5394	MINQ_S	0x18	RW	Bit[6:0]: Minimum Q for auto Q when gain larger than maxgain, for S
0x5395	MAXQ_S	0x40	RW	Bit[6:0]: Maximum Q for auto Q when gain smaller than mingain, for S
0x5396	BR_HSCALE_S_ BYTE1	0x02	RW	Bit[2:0]: H scale for blue/red channel for S[10:8]
0x5397	BR_HSCALE_S_ BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for S[7:0]
0x5398	BR_VSCALE_S_ BYTE1	0x02	RW	Bit[2:0]: V scale for blue/red channel for S[10:8]
0x5399	BR_VSCALE_S_ BYTE0	0xF4	RW	Bit[7:0]: V scale for blue/red channel for S[7:0]

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table 4-3 LENC control registers (sheet 18 of 18)

address	register name	default value	R/W	description
0x539A	G_HSCALE_S_ BYTE1	0x02	RW	Bit[2:0]: H scale for blue/red channel for S[10:8]
0x539B	G_HSCALE_S_ BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for S[7:0]
0x539C	G_VSCALE_S_ BYTE1	0x01	RW	Bit[2:0]: V scale for blue/red channel for S[10:8]
0x539D	G_VSCALE_S_ BYTE0	0x7A	RW	Bit[7:0]: V scale for blue/red channel for S[7:0]
0x539E	BR_HSCALE_VS_ BYTE1	0x02	RW	Bit[2:0]: H scale for blue/red channel for VS[10:8]
0x539F	BR_HSCALE_VS_ BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for VS[7:0]
0x53A0	BR_VSCALE_VS_ BYTE1	0x02	RW	Bit[2:0]: V scale for blue/red channel for VS[10:8]
0x53A1	BR_VSCALE_VS_ BYTE0	0xF4	RW	Bit[7:0]: V scale for blue/red channel for VS[7:0]
0x53A2	G_HSCALE_VS_ BYTE1	0x02	RW	Bit[2:0]: H scale for blue/red channel for VS[10:8]
0x53A3	G_HSCALE_VS_ BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for VS[7:0]
0x53A4	G_VSCALE_VS_ BYTE1	0x01	RW	Bit[2:0]: V scale for blue/red channel for VS[10:8]
0x53A5	G_VSCALE_VS_ BYTE0	0x7A	RW	Bit[7:0]: V scale for blue/red channel for VS[7:0]
0x53A6~ 0x53A8	RSVD	–	–	Reserved
0x53A9	M_NQ_L	–	R	Bit[6:0]: m_nQ effective for L
0x53AA	M_NQ_S	–	R	Bit[6:0]: m_nQ effective for S
0x53AB	M_NQ_VS	–	R	Bit[6:0]: m_nQ effective for VS

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4.3 auto white balance (AWB)

The next process in the pipeline is white balance. The RAW R, G and B values of a gray object vary with the spectrum of the illumination and the sensor spectral response. Illumination spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray, the sensor needs to adjust the gain for each color channel according to color temperature. This process is called white balance (WB).

White balance gain is enabled by default and can be disabled in register 0x5000[1]. The applied WB gain can be read back from register 0x5080~0x5097 and offset values can be read back from registers 0x5099~0x50C7.

4.3.1 WB gain

The WB gain to be applied can be selected by register 0x5000[5]. When this register is set to 0, the values from registers 0x5770~0x5777, 0x5778~0x577F and 0x5780~0x5787 are selected for long, short and very short channel WB gain, respectively. When this bit is set to 1, the internal gain calculated by the auto white balance (AWB) algorithm is selected and the gain is also written back to registers 0x5080~0x5097.

The maximum WB gain is set by registers 0x5700~0x5705

table 4-4 AWB control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP RW00	0xFB	RW	Bit[5]: AWB gain manual 0: AWB gain adjusted automatically 1: AWB gain adjusted by user Bit[1]: AWB gain enable 0: Disable 1: Enable
0x5080~0x5081	AWBRGAIN_L	0x128	RW	Long Channel Red Gain
0x5082~0x5083	AWBGRGAIN_L	0x100	RW	Long Channel Gr Gain
0x5084~0x5085	AWBGBGAIN_L	0x100	RW	Long Channel Gb Gain
0x5086~0x5087	AWBBGAIN_L	0x200	RW	Long Channel Blue Gain
0x5088~0x5089	AWBRGAIN_S	0x128	RW	Short Channel Red Gain
0x508A~0x508B	AWBGRGAIN_S	0x100	RW	Short Channel Gr Gain

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table 4-4 AWB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x508C~ 0x508D	AWBGBGAIN_S	0x100	RW	Short channel Gb Gain
0x508E~ 0x508F	AWBBGAIN_S	0x200	RW	Short channel Blue Gain
0x5090~ 0x5091	AWBRGAIN_VS	0x128	RW	Very Short Channel Red Gain
0x5092~ 0x5093	AWBGRGAIN_VS	0x100	RW	Very Short Channel Gr Gain
0x5094~ 0x5095	AWBGBGAIN_VS	0x100	RW	Very Short Channel Gb Gain
0x5096~ 0x5097	AWBBGAIN_VS	0x200	RW	Very Short Channel Blue Gain
0x5700~ 0x5701	AWB_MAX_RGAIN	–	–	Maximum Red WB Gain
0x5702~ 0x5703	AWB_MAX_GGAIN	–	–	Maximum Green WB Gain
0x5704~ 0x5705	AWB_MAX_BGAIN	–	–	Maximum Blue WB Gain
0x5770~ 0x5771	MANUALAWBRGAIN_L	–	–	Long Channel Red Manual Gain
0x5772~ 0x5773	MANUALAWBGRGAIN_L	–	–	Long Channel Gr Manual Gain
0x5774~ 0x5775	MANUALAWBGBGAIN_L	–	–	Long Channel Gb Manual Gain
0x5776~ 0x5777	MANUALAWBBGAIN_L	–	–	Long Channel Blue Manual Gain
0x5778~ 0x5779	MANUALAWBRGAIN_S	–	–	Short Channel Red Manual Gain
0x577A~ 0x577B	MANUALAWBGRGAIN_S	–	–	Short Channel Gr Manual Gain
0x577C~ 0x577D	MANUALAWBGBGAIN_S	–	–	Short Channel Gb Manual Gain
0x577E~ 0x577F	MANUALAWBBGAIN_S	–	–	Short Channel Blue Manual Gain
0x5780~ 0x5781	MANUALAWBRGAIN_VS	–	–	Very Short Channel Red Manual Gain
0x5782~ 0x5783	MANUALAWBGRGAIN_VS	–	–	Very Short Channel Gr Manual Gain

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table 4-4 AWB control registers (sheet 3 of 3)

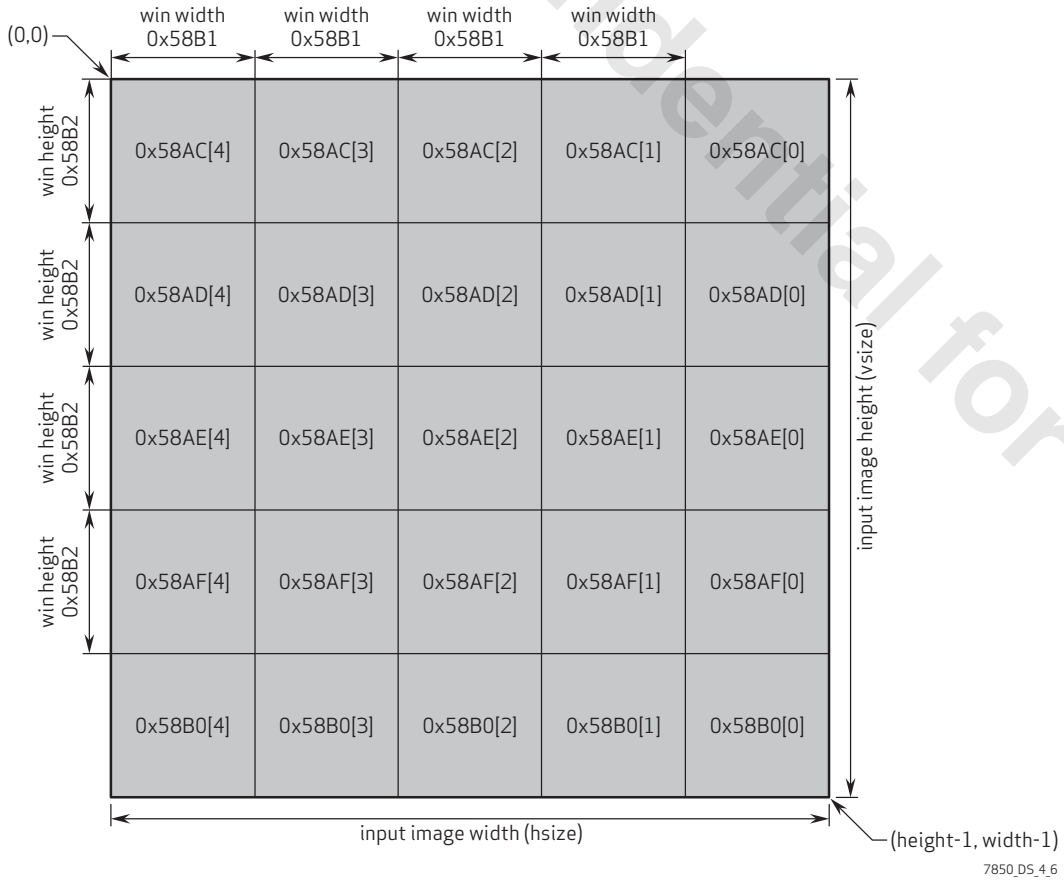
address	register name	default value	R/W	description
0x5784~ 0x5785	MANUALAWBGBGAIN_VS	–	–	Very Short Channel Gb Manual Gain
0x5786~ 0x5787	MANUALAWBBGAIN_VS	–	–	Very Short Channel Blue Manual Gain

4.3.2 AWB statistics

AWB region-of-interest (ROI) is controlled by a programmable rectangular window and a 5x5 block of the input image.

The image is divided into a 5x5 block for AWB statistics calculation. The width and height of the top-left 4x4 block is defined by registers 0x58B1 and 0x58B2, respectively. The user can define whether each block is included or excluded from the statistics calculation with registers 0x58AC~0x58B0, respectively (see **figure 4-6**).

figure 4-6 advanced AWB diagram



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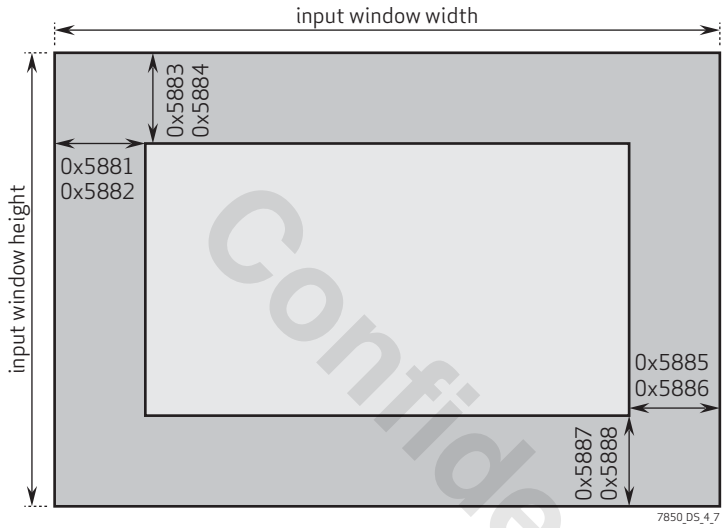
For the block included in the AWB statistics calculation, the pixel is further adjusted by the rectangular window (see **figure 4-7**). The window location and size are defined by register 0x5881~0x5888. This ROI window is enabled by register 0x5880[1]. When it is enabled, pixels outside are excluded from AWB statistics.

figure 4-7 AWB ROI position diagram



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Too dark or bright pixels are excluded from the statistics. Pixels with a value (in 10-bit scale) greater than registers {0x588A[7:0], 0x588B[7:0]} or less than registers {0x588C[7:0], 0x588D[7:0]} are excluded from the statistics.

The more number of gray pixels in the scene, the more accurate the AWB is. In order to increase AWB accuracy, the sensor starts to adjust WB gain only when gray pixel number exceeds certain threshold. The threshold is defined by registers {0x5714[7:0], 0x5715[7:0]}.

AWB statistics can be calculated from the sub-sampled image. The horizontal and vertical sub-sampling ratio is set by registers 0x5889[3:2] and 0x5889[1:0], respectively.

table 4-5 advanced AWB control registers (sheet 1 of 3)

address	register name	default value	R/W	description	
0x5880	R_ADVANCED_AWB_CTRL	0x04	RW	Bit[1]:	Curve AWB statistic ROI enable
0x5881	R_STAT_RECT_LEFT_H	0x00	RW	Bit[1:0]:	Statistic ROI left coordinate[9:8]
0x5882	R_STAT_RECT_LEFT_L	0x10	RW	Bit[7:0]:	Statistic ROI left coordinate[7:0]
0x5883	R_STAT_RECT_TOP_H	0x00	RW	Bit[1:0]:	Statistic ROI top coordinate[9:8]
0x5884	R_STAT_RECT_TOP_L	0x10	RW	Bit[7:0]:	Statistic ROI top coordinate[7:0]
0x5885	R_STAT_RECT_RIGHT_H	0x02	RW	Bit[1:0]:	Statistic ROI right coordinate[9:8]

table 4-5 advanced AWB control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5886	R_STAT_RECT_RIGHT_L	0x6C	RW	Bit[7:0]: Statistic ROI right coordinate[7:0]
0x5887	R_STAT_RECT_BOTTOM_H	0x01	RW	Bit[1:0]: Statistic ROI bottom coordinate[9:8]
0x5888	R_STAT_RECT_BOTTOM_L	0xC8	RW	Bit[7:0]: Statistic ROI bottom coordinate[7:0]
0x5889	R_STATISTIC_RATE	0x44	RW	Bit[7:4]: X direction statistics rate Bit[3:0]: Y direction statistics rate
0x588A	R_MAX_VALUE_H	0x03	RW	Bit[1:0]: Statistic max value[9:8]
0x588B	R_MAX_VALUE_L	0xE0	RW	Bit[7:0]: Statistic max value[7:0]
0x588C	R_MIN_VALUE_H	0x00	RW	Bit[1:0]: Statistic min value[9:8]
0x588D	R_MIN_VALUE_L	0x0E	RW	Bit[7:0]: Statistic min value[7:0]
0x5892	R_SCALE_BITS	0x0A	RW	Bit[3:0]: Scale bits
0x5714	AWBMINNUM_H	0x04	RW	AWB Minimum Statistics Number High Byte
0x5715	AWBMINNUM_L	0x00	RW	AWB Minimum Statistics Number Low Byte
0x5893	R_WEIGHT_TH	0x00	RW	Bit[7:0]: Weight threshold
0x58AC	R_ROW0_WIN_EN	0x1F	RW	Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable
0x58AD	R_ROW1_WIN_EN	0x1F	RW	Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x58AE	R_ROW2_WIN_EN	0x1F	RW	Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x58AF	R_ROW3_WIN_EN	0x1F	RW	Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable

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table 4-5 advanced AWB control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x58B0	R_ROW4_WIN_EN	0x1F	RW	Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable
0x58B1	R_SUB_WIN_WIDTH	0x96	RW	Bit[7:0]: Sub-window width
0x58B2	R_SUB_WIN_HEIGHT	0x68	RW	Bit[7:0]: Sub-window height

4.3.3 AWB gain mode

The OV7850 applies the gain obtained from the long channel image to long, short, and very short channel. The very short channel is captured by the same sub-pixel as the long channel, so the AWB gain is the same as the long channel. The spectral response of the short channel sub-pixel is not identical to long channel due to different pixel size, so the AWB gain obtained from long channel cannot be directly applied to the short channel. To compensate the difference, a programmable ratio is applied on the long channel gain to derive the gain for short channel. This feature is enabled by register 0x5740[0]. The B/G gain ratio is set by registers {0x574C[7:0], 0x574D[7:0]} and {0x5752[7:0], 0x5753[7:0]}. The R/G gain ratio is set by registers {0x5758[7:0], 0x5759[7:0]} and {0x5752[7:0], 0x5753[7:0]}. The ratio is adaptive to color temperature, which can be enabled by register 0x5741[0]. Color temperature is defined as 128*B/R, here B and R are AWB gain at different color temperatures. Registers {0x5742[7:0], 0x5743[7:0]} are for Day light threshold. Registers {0x5744[7:0], 0x5745[7:0]} are for CWF light threshold. Registers {0x5746[7:0], 0x5747[7:0]} are for A light threshold.

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figure 4-8 AWB gain mode diagram

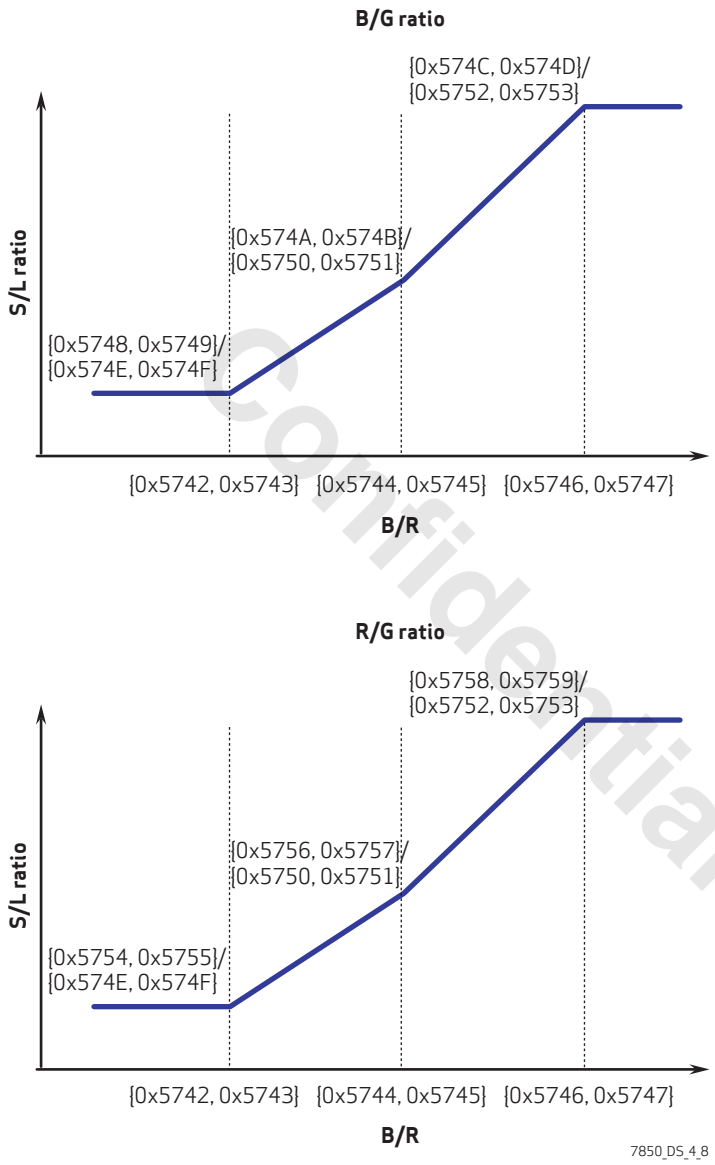

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table 4-6 AWB gain mode registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5880	AWB GAIN MODE	0x04	RW	Bit[4:3]: AWB gain mode 00: Long mode Both long and short channel AWB gain are based on long channel statistics 01: Not used 1x: Not used
0x5740	ADJUSTSMALLPDGAIN ENABLE	–	–	Adjust Short Channel AWB Gain Enable
0x5741	ADAPTIVEPDGAIN ENABLE	–	–	Adaptive Short Channel AWB Gain Enable
0x5742	BRGAINTH_0_H	–	–	BRGainTh_0_h
0x5743	BRGAINTH_0_L	–	–	BRGainTh_0_l
0x5744	BRGAINTH_1_H	–	–	BRGainTh_1_h
0x5745	BRGainTh_1_l	–	–	BRGainTh_1_l
0x5746	BRGainTh_2_h	–	–	BRGainTh_2_h
0x5747	BRGainTh_2_l	–	–	BRGainTh_2_l
0x5748	PDGAINB_0_H	–	–	BlueGain_0_h
0x5749	PDGAINB_0_L	–	–	BlueGain_0_l
0x574A	PDGAINB_1_H	–	–	BlueGain_1_h
0x574B	PDGAINB_1_L	–	–	BlueGain_1_l
0x574C	PDGAINB_2_H	–	–	BlueGain_2_h
0x574D	PDGAINB_2_L	–	–	BlueGain_2_l
0x574E	PDGAING_0_H	–	–	GreenGain_0_h
0x574F	PDGAING_0_L	–	–	GreenGain_0_l
0x5750	PDGAING_1_H	–	–	GreenGain_1_h
0x5751	PDGAING_1_L	–	–	GreenGain_1_l
0x5752	PDGAING_2_H	–	–	GreenGain_2_h
0x5753	PDGAING_2_L	–	–	GreenGain_2_l
0x5754	PDGAINR_0_H	–	–	RedGain_0_h
0x5755	PDGAINR_0_L	–	–	RedGain_0_l
0x5756	PDGAINR_1_H	–	–	RedGain_1_h

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table 4-6 AWB gain mode registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5757	PDGAINR_1_L	–	–	RedGain_1_l
0x5758	PDGAINR_2_H	–	–	RedGain_2_h
0x5759	PDGAINR_2_L	–	–	RedGain_2_l

4.3.4 AWB algorithm

The AWB algorithm works in either simple or advanced mode. The AWB algorithm can be also disabled and the WB gains are fully controlled by the backend processor.

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table 4-7 AWB algorithm register

address	register name	default value	R/W	description
0x5880	AWB_CTRL01	0x04	RW	Bit[2]: Advance temperature AWB Algorithms enable 0: Disable 1: Enable

4.3.5 speed and stable range

From the white balance state, the AWB algorithm will start to adjust the WB gain again once the difference between color channels is greater than threshold set by register 0x587A/0x100. The AWB algorithm will keep adjusting them until the difference is less than the threshold set by register 0x5879/0x100.

Register 0x575A is the relative WB gain adjustment step, which determines WB gain adjustment based on the distance from current WB gain to target WB gain. Register 0x575B sets the maximum number of adjustments the algorithm will take before stopping.

table 4-8 AWB stable range registers

address	register name	default value	R/W	description
0x575A	AWB_STEP_1	–	–	Relative AWB Adjustment Step
0x575B	AWB_STEP_2	–	–	Maximum Number of Adjustments
0x5879	AWB_STABLE_RG_1	–	–	AWB Stable Range 1
0x587A	AWB_STABLE_RG_2	–	–	AWB Stable Range 2

4.3.6 simple AWB algorithm

Simple AWB algorithm is based on the Gray World assumption, meaning the sensor will make the R, G, and B average of all pixels equal to each other by adjusting the gain of each color channel. This is accomplished by taking the statistics of all pixels.

4.3.7 advanced AWB algorithm

Advanced AWB algorithm adjusts the R, G, and B gain based on the color temperature of the ambient light.

To identify a gray object over the color temperature range, the AWB algorithm must know the WB gain in order to achieve good white balance for a gray object with the target lens in the illumination of the entire interested color temperature range. These WB gains form an irregular area in the blue-red gain space as shown in **figure 4-8**, where the red and blue gain has been normalized by green gain.

Finding the gain area for the entire color temperature range is time consuming, complicated and prone to error. To simplify this process, the algorithm takes the normalized red and blue gain in representative low, middle, and high color temperature illumination, and automatically extends them to define the gain area, as shown in **figure 4-8**.

The gain area is divided into a 16x16 block, and the user can define the weighting of each block. The weighting of each block represents the likelihood of the corresponding color temperature appearing in the real world. The user can exclude some blocks by assigning 0 weighting to fine tune the gain area. It is also possible to prevent color wash out from a solid color object, skin, etc. by properly defining the weighting to exclude them from the gain area.

Registers 0x57A7~0x5826 define the weighting of the 256 blocks. The weight ranges from 0x0 to 0x0F. The higher the weighting, the more emphasis on that color temperature. Natural lighting (e.g., outdoors on a sunny day) usually spans a certain range, so it is better to avoid big weight changes between the adjacent blocks.

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figure 4-9 advanced AWB algorithm diagram

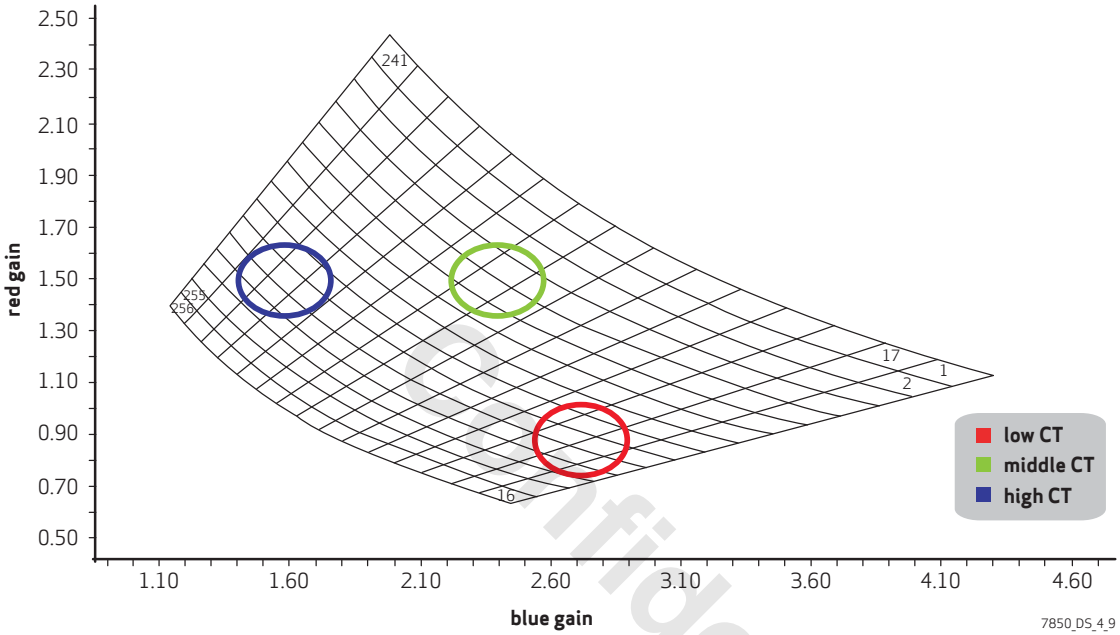

table 4-9 AWB weight registers

address	register name	default value	R/W	description
0x57A7	AWB_WEIGHT_1_2	–	–	Bit[7:4]: Sub-window1 weight Bit[3:0]: Sub-window2 weight
0x57A8	AWB_WEIGHT_3_4	–	–	Bit[7:4]: Sub-window3 weight Bit[3:0]: Sub-window4 weight
0x57A9~ 0x5825	AWB_WEIGHT_3_252	–	–	Weight From Sub-window3 to Sub-window252
0x5826	AWB_WEIGHT_253_254	–	–	Bit[7:4]: Sub-window253 weight Bit[3:0]: Sub-window254 weight
0x5827	AWB_WEIGHT_255_256	–	–	Bit[7:4]: Sub-window255 weight Bit[3:0]: Sub-window256 weight

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4.3.8 advanced AWB tuning guidelines

The AWB control parameters must be calibrated using the target lens because the lens spectral transmittance affects the color ratio.

The lens correction profile will also slightly change the overall color ratio. So, lens shading correction has to be fine tuned before AWB tuning.

Tuning the AWB in a light box with low, middle, and high color temperature illuminator is the fastest way to achieve the correct setting. Either the WB gain, to achieve good white balance for a gray scene, or the raw images, that contain some gray object without WB gain, can be used to determine the advanced AWB parameters.

However, the R, G, and B gain in various lighting conditions with good white balance (by either manual adjustment, or by simple AWB with a neutral scene) are helpful for checking and improving the AWB setting coverage.

The WB gain of artificial light can vary by large amounts. It is important to check the WB gain in these conditions if the target application is required to run in these lighting conditions.

There is a trade off between the AWB accuracy and the coverage. A smaller WB gain area provides more accurate WB result, but the coverage is lower and the AWB may fail in certain light conditions.

4.3.9 post AWB gain

In advanced AWB mode, after the WB gain is calculated from the AWB statistics, a programmable value can be added to shift the color. These values are programmable through registers 0x57A0~0x57A6 for each color of the long channel.

Registers 0x5080~0x5087 are the gain values after this adjustment.

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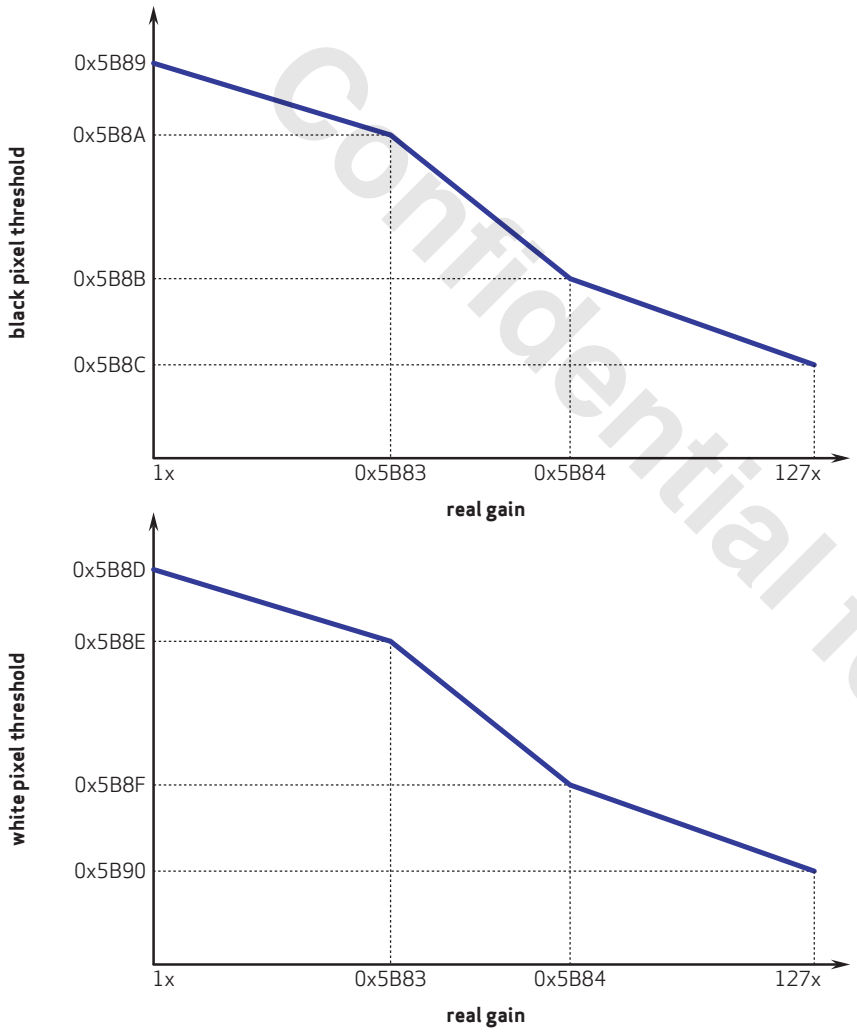
table 4-10 advanced AWB control registers

address	register name	default value	R/W	description
0x57A0	BGAINSHIFT_H	–	–	Long Channel Blue Gain Adjustment High Byte BGain = BGain × BGainShift / 128
0x57A1	BGAINSHIFT_L	–	–	Long Channel Blue Gain Adjustment Low Byte
0x57A2	GGAINSHIFT_H	–	–	Long Channel Green Gain Adjustment High Byte GGain = GGain × GGainShift / 128
0x57A3	GGAINSHIFT_L	–	–	Long Channel Green Gain Adjustment Low Byte
0x57A4	RGAINSHIFT_H	–	–	Long Channel Red Gain Adjustment High Byte RGain = RGain × RGainShift / 128
0x57A5	RGAINSHIFT_L	–	–	Long Channel Red Gain Adjustment Low Byte
0x57A6	SHIFT_ENABLE	–	–	Enable Post AWB Gain When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.

4.4 defect pixel correction (DPC)

The DPC function detects defect pixels/cluster by using a programmable threshold. The threshold can be automatically calculated based on analog gain from a programmable threshold gain curve or set manually by register 0x5B80[0]. Refer to **figure 4-10** for details, where the "channel" means L, S or VS channel. In the OV7850, the DPC module is enabled/disabled with same signal for L/S/VS channels 0x5001[4:3], but white/black defect pixel process can be set with different value for L/S/VS channels.

figure 4-10 threshold gain curve in auto threshold mode



note 1x < DPC_gain_thre1 < DPC_gain_thre2<128x
white_thre0 > white_thre1> white_thre2 > white_thre3
black_thre0 > black_thre1> black_thre2> black_thre3

7850_DS_4_10

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The DPC can correct single defect pixels, couplets, cross types and tail types. The following figures illustrate defect patterns that can be detected. Refer to registers 0x5B80~0x5BF for more detailed information about DPC configuration.

figure 4-11 types of white pixels

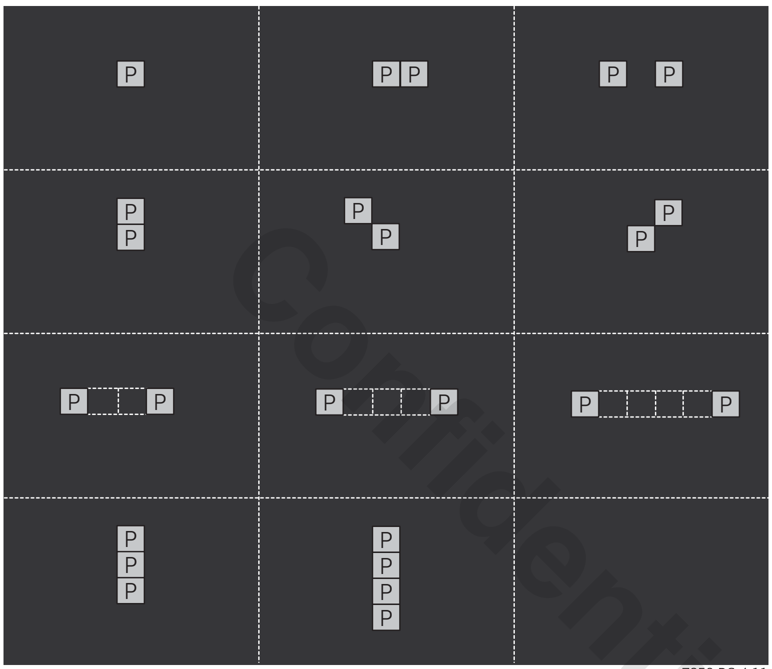

figure 4-12 example of different channel connected

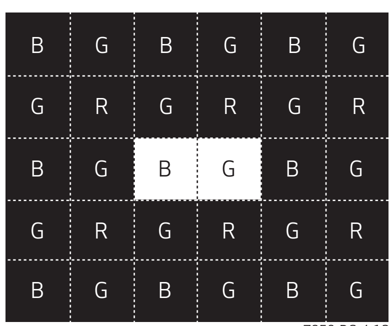

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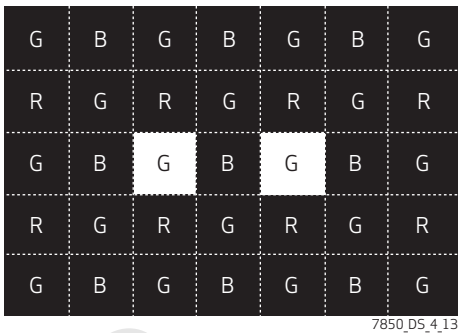
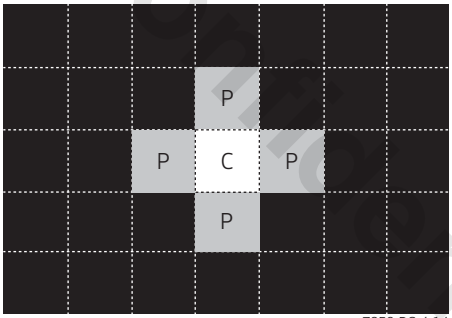
figure 4-13 example of same channel connected



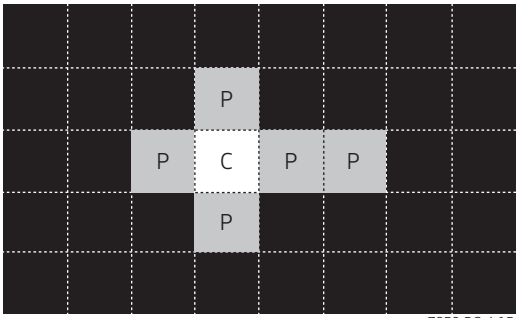
7850_DS_4_13

figure 4-14 example of white cluster



7850_DS_4_14

figure 4-15 example of tailing pixel



7850_DS_4_15

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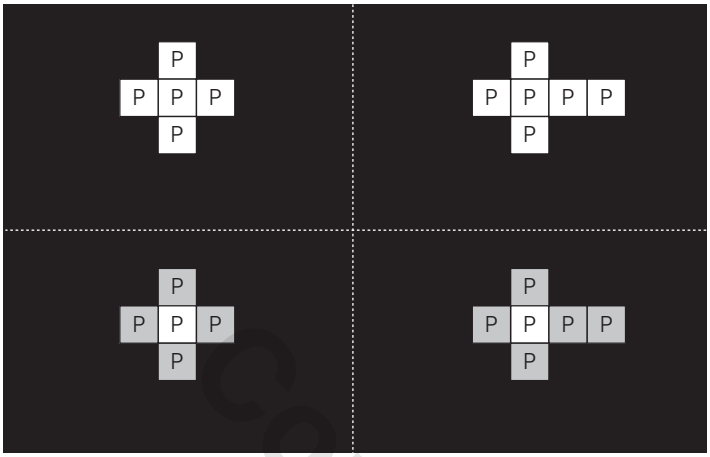
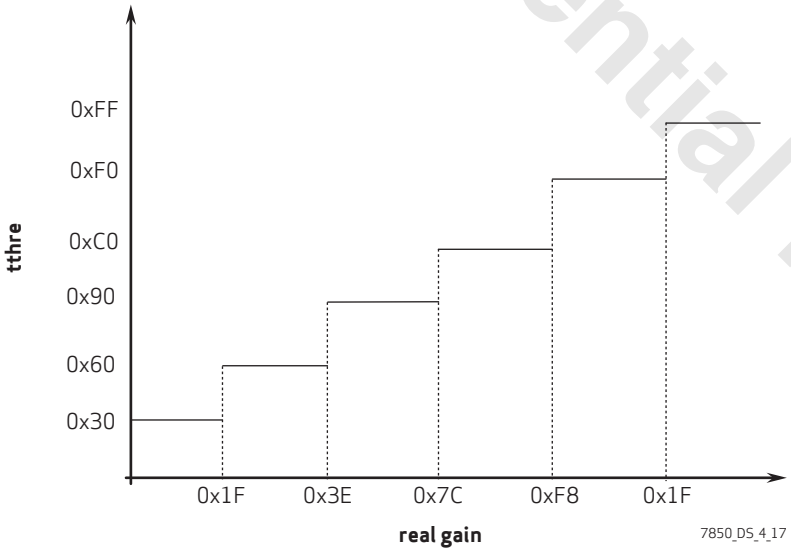
figure 4-16 example of tailing pixel



Threshold for T-cluster can be manually set or changed automatically according to real gain, register 0x5B81[7], see **figure 4-17**.

figure 4-17 threshold for T-cluster diagram



If vertical black pixel detection is enabled (0x5B81[5]), it is automatically activated by relationship between sensor real gain and a thresholds set by registers 0x5B92, 0x5B93.

- activated if ({0x5B92}+1)×16 is less than sensor real gain
- deactivated if ({0x5B93}+1)×16 higher than sensor real gain

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table 4-11 DPC control registers (sheet 1 of 12)

address	register name	default value	R/W	description
0x5B80	R_L_DPC_CTRL00	0x18	RW	For Long Exposure Channel Bit[7]: Tail type cross cluster correction enable, works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable, works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 4-11 DPC control registers (sheet 2 of 12)

address	register name	default value	R/W	description
0x5B81	R_L_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5B82	R_L_DPC_CTRL02	0xFF	RW	For Long Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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table 4-11 DPC control registers (sheet 3 of 12)

address	register name	default value	R/W	description
0x5B83	R_L_WTHREGLIST1	0x08	RW	For Long Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5B84	R_L_WTHREGLIST2	0x20	RW	For Long Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5B85	R_L_THRE1	0x10	RW	For Long Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but less effective of recovering defect
0x5B86	R_L_THRE2	0x20	RW	For Long Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5B87	R_L_THRE3	0x10	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine high frequency area where DPC will keep fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5B88	R_L_THRE4	0x18	RW	For Long Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than threshold for single white/black pixel
0x5B89	R_L_WTHRE_LIST0	0x08	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode
0x5B8A	R_L_WTHRE_LIST1	0x04	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x5B8B	R_L_WTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode

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table 4-11 DPC control registers (sheet 4 of 12)

address	register name	default value	R/W	description
0x5B8C	R_L_WTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x5B8D	R_L_BTHRE_LIST0	0x0C	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 0 in auto mode
0x5B8E	R_L_BTHRE_LIST1	0x06	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 1 in auto mode
0x5B8F	R_L_BTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 2 in auto mode
0x5B90	R_L_BTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[6:0]: Black pixel threshold 3 in auto mode
0x5B91	R_L_SAT	0xFF	RW	For Long Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5B92	R_L_VB_GAIN_TH1	0x07	RW	For Long Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x5B93	R_L_VB_GAIN_TH2	0x03	RW	For Long Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x5B94	R_L_SMOOTH_ GLIST0	0x03	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 0
0x5B95	R_L_SMOOTH_ GLIST1	0x07	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 1
0x5B96	R_L_SMOOTH_ GLIST2	0x0F	RW	For Long Exposure Channel Bit[6:0]: Smooth gain list 2
0x5B97~ 0x5B98	NOT USED	–	–	Not Used
0x5B99	R_L_UNSAT	0xF0	RW	For Long Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5B9A	R_L_TTHRE	0x08	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

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table 4-11 DPC control registers (sheet 5 of 12)

address	register name	default value	R/W	description
0x5BA0	R_S_DPC_CTRL00	0x18	RW	For Short Exposure Channel Bit[7]: Tail type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 4-11 DPC control registers (sheet 6 of 12)

address	register name	default value	R/W	description
0x5BA1	R_S_DPC_CTRL01	0xDF	RW	For Short Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5BA2	R_S_DPC_CTRL02	0xFF	RW	For Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed: 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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table 4-11 DPC control registers (sheet 7 of 12)

address	register name	default value	R/W	description
0x5BA3	R_S_WTHREGLIST1	0x08	RW	For Short Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5BA4	R_S_WTHREGLIST2	0x20	RW	For Short Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5BA5	R_S_THRE1	0x10	RW	For Short Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but less effective of recovering defect
0x5BA6	R_S_THRE2	0x20	RW	For Short Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5BA7	R_S_THRE3	0x10	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where DPC will keep fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5BA8	R_S_THRE4	0x18	RW	For Short Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than threshold for single while/black pixel
0x5BA9	R_S_WTHRE_LIST0	0x08	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode
0x5BAA	R_S_WTHRE_LIST1	0x04	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x5BAB	R_S_WTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode

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table 4-11 DPC control registers (sheet 8 of 12)

address	register name	default value	R/W	description
0x5BAC	R_S_WTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x5BAD	R_S_BTHRE_LIST0	0x0C	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 0 in auto mode
0x5BAE	R_S_BTHRE_LIST1	0x06	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 1 in auto mode
0x5BAF	R_S_BTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 2 in auto mode
0x5BB0	R_S_BTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[6:0]: Black pixel threshold 3 in auto mode
0x5BB1	R_S_SAT	0xFF	RW	For Short Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5BB2	R_S_VB_GAIN_TH1	0x07	RW	For Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x5BB3	R_S_VB_GAIN_TH2	0x03	RW	For Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x5BB4	R_S_SMOOTH_ GLIST0	0x03	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 0
0x5BB5	R_S_SMOOTH_ GLIST1	0x07	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 1
0x5BB6	R_S_SMOOTH_ GLIST2	0x0F	RW	For Short Exposure Channel Bit[6:0]: Smooth gain list 2
0x5BB7~ 0x5BB8	NOT USED	–	–	Not Used
0x5BB9	R_S_UNSAT	0xF0	RW	For Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5BBA	R_S_TTHRE	0x08	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster

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table 4-11 DPC control registers (sheet 9 of 12)

address	register name	default value	R/W	description
0x5BC0	R_VS_DPC_CTRL00	0x18	RW	For Very Short Exposure Channel Bit[7]: Tail type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table 4-11 DPC control registers (sheet 10 of 12)

address	register name	default value	R/W	description
0x5BC1	R_VS_DPC_CTRL01	0xDF	RW	For Very Short Exposure Channel Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5BC2	R_VS_DPC_CTRL02	0xFF	RW	For Very Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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table 4-11 DPC control registers (sheet 11 of 12)

address	register name	default value	R/W	description
0x5BC3	R_VS_WTHREG LIST1	0x08	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5BC4	R_VS_WTHREG LIST2	0x20	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5BC5	R_VS_THRE1	0x10	RW	For Very Short Exposure Channel Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but less effective of recovering defect
0x5BC6	R_VS_THRE2	0x20	RW	For Very Short Exposure Channel Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5BC7	R_VS_THRE3	0x10	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where DPC will keep fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5BC8	R_VS_THRE4	0x18	RW	For Very Short Exposure Channel Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x5BC9	R_VS_WTHRE_ LIST0	0x08	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 0 in auto mode
0x5BCA	R_VS_WTHRE_ LIST1	0x04	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 1 in auto mode
0x5BCB	R_VS_WTHRE_ LIST2	0x02	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 2 in auto mode

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table 4-11 DPC control registers (sheet 12 of 12)

address	register name	default value	R/W	description
0x5BCC	R_VS_WTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[6:0]: White pixel threshold 3 in auto mode
0x5BCD	R_VS_BTHRE_LIST0	0x0C	RW	For Very Short Exposure Channel Bit[6:0]: Black pixel threshold 0 in auto mode
0x5BCE	R_VS_BTHRE_LIST1	0x06	RW	For Very Short Exposure Channel Bit[6:0]: Black pixel threshold 1 in auto mode
0x5BCF	R_VS_BTHRE_LIST2	0x02	RW	For Very Short Exposure Channel Bit[6:0]: Black pixel threshold 2 in auto mode
0x5BD0	R_VS_BTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[6:0]: Black pixel threshold 3 in auto mode
0x5BD1	R_VS_SAT	0xFF	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5BD2	R_VS_VB_GAIN_TH1	0x07	RW	For Very Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 1
0x5BD3	R_VS_VB_GAIN_TH2	0x03	RW	For Very Short Exposure Channel Bit[6:0]: Vertical black pixel detection threshold 2
0x5BD4	R_VS_SMOOTH_GLIST0	0x03	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 0
0x5BD5	R_VS_SMOOTH_GLIST1	0x07	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 1
0x5BD6	R_VS_SMOOTH_GLIST2	0x0F	RW	For Very Short Exposure Channel Bit[6:0]: Smooth gain list 2
0x5BD7~ 0x5BD8	NOT USED	–	–	Not Used
0x5BD9	R_VS_UNSAT	0xF0	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5BDA	R_VS_TTHRE	0x08	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x5BE0~ 0x5BF7	RSVD	–	–	Reserved

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4.5 de-noise (DNS)

There are several steps to reduce the noise in OV7850 image pipeline and each de-noise stage is designed to reduce different noise. Based on their stages in the pipeline, they can be classified into two classes: linear domain DNS and after gamma DNS.

RAWDNS is the first step in linear domain DNS. Because the AWB gain often amplifies the noise in R/B channels, the RAWDNS is mainly designed to reduce noise in R/B channel before color interpolation. It also supports to reduce noise in green channel, but this may remove too much detail and may cause blurry images. So unless the sensor noise is very large, it is not recommended to reduce green channel noise in RAWDNS.

CIP is the second step in linear domain DNS, which is designed to reduce noise in green channel during color interpolation. Because CIP is edge adaptive, it can keep sharp edges better than the de-noising of green channel in RAWDNS.

Because the color matrix and gamma curve will amplify the noise, which is mainly in low frequency after the linear domain DNS. The gamma DNS modules (UVDNS) is designed to remove low frequency Y and UV noise. UVDNS is the second step DNS after gamma, which is designed to reduce UV noise.

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4.5.1 noise list

The noise level increases with sensor AGC gain, so the DNS modules will also need to increase de-noise level with gain. All these four modules have the same logic to auto adjust de-noise level with sensor AGC gain: an 8-step noise list, which defines the de-noise level will be used when the sensor AGC gain is x1, x2, x4, x8, x16, x32, x64 or x128. If the AGC gain is between two steps, the real de-noise level will be linear interpolated between two steps. Each DNS modules has its own noise list.

Besides the noise list, different modules still have different controls. The RAWDNS and UVDNS will be introduced in the following sections. The DNS in CIP will be discussed in **section 4.9,** color interpolation (CIP).

4.5.2 RAWDNS

In RAWDNS, except for the noise list, there are three parameters, which can influence image quality.

1. green channel de-noising

   There is an option for choosing G position pixels to be involved in de-noise, enabled by registers 0x5108, 0x5113, 0x511E for L, S and VS, respectively. Note that enabling the green channel de-noising may remove image details and result in a blurry image. Unless the sensor noise level is very high, it is recommended to disable green channel de-noising.

2. noise Y slop signal

   There is an option to increase the DNS level with the signal level, adjusted by registers 0x5109, 0x5114 and 0x511F for L, S and VS respectively. In linear domain, the shot noise increase with signal level, so for a linear raw image, the dark tone has lower noise level than mid tone and light tone. A larger value will reduce more noise in light tone.

3. maximum edge threshold

   There is an option to preserve color edges in low light conditions, adjusted by registers 0x510A, 0x5115 and 0x5120 for L, S and VS respectively. A smaller value will preserve color edges, but also remove less noise in R/B channels.

table 4-12 HDR_RAW control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5100	R_NOISELIST0_L_I	0x01	RW	Bit[7:0]: NoiseList0 for L exposure channel RAW de-noise
0x5101	R_NOISELIST1_L_I	0x02	RW	Bit[7:0]: NoiseList1 for L exposure channel RAW de-noise
0x5102	R_NOISELIST2_L_I	0x04	RW	Bit[7:0]: NoiseList2 for L exposure channel RAW de-noise
0x5103	R_NOISELIST3_L_I	0x08	RW	Bit[7:0]: NoiseList3 for L exposure channel RAW de-noise
0x5104	R_NOISELIST4_L_I	0x0C	RW	Bit[7:0]: NoiseList4 for L exposure channel RAW de-noise
0x5105	R_NOISELIST5_L_I	0x10	RW	Bit[7:0]: NoiseList5 for L exposure channel RAW de-noise
0x5106	R_NOISELIST6_L_I	0x12	RW	Bit[7:0]: NoiseList6 for L exposure channel RAW de-noise
0x5107	R_NOISELIST7_L_I	0x18	RW	Bit[7:0]: NoiseList7 for L exposure channel RAW de-noise
0x5108	R_G_DNS_EN_L_I	0x01	RW	Bit[0]: Green channel de-noising for L channel 0: Disable 1: Enable
0x5109	R_NOISE_YSLOP _L_I	0x04	RW	Bit[3:0]: Noise Y slop signal for L channel
0x510A	R_MAX_EDGE_THRE _L_I	0x3F	RW	Bit[7:0]: Maximum edge threshold for L channel
0x510B	R_NOISELIST0_S_I	0x04	RW	Bti[7:0]: NoiseList0 for S exposure channel RAW de-noise
0x510C	R_NOISELIST1_S_I	0x08	RW	Bit[7:0]: NoiseList1 for S exposure channel RAW de-noise
0x510D	R_NOISELIST2_S_I	0x10	RW	Bit[7:0]: NoiseList2 for S exposure channel RAW de-noise
0x510E	R_NOISELIST3_S_I	0x18	RW	Bit[7:0]: NoiseList3 for S exposure channel RAW de-noise
0x510F	R_NOISELIST4_S_I	0x20	RW	Bit[7:0]: NoiseList4 for S exposure channel RAW de-noise
0x5110	R_NOISELIST5_S_I	0x30	RW	Bit[7:0]: NoiseList5 for S exposure channel RAW de-noise
0x5111	R_NOISELIST6_S_I	0x40	RW	Bit[7:0]: NoiseList6 for S exposure channel RAW de-noise

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table 4-12 HDR_RAW control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5112	R_NOISELIST7_S_I	0x40	RW	Bit[7:0]: NoiseList7 for S exposure channel RAW de-noise
0x5113	R_G_DNS_EN_S_I	0x01	RW	Bit[0]: Green channel de-noising for S channel 0: Disable 1: Enable
0x5114	R_NOISE_YSLOP _S_I	0x04	RW	Bit[3:0]: Noise Y slop signal S channel
0x5115	R_MAX_EDGE_THRE _S_I	0x3F	RW	Bit[7:0]: Maximum edge threshold S channel
0x5116	R_NOISELIST0_V_I	0x04	RW	Bit[7:0]: NoiseList0 for VS exposure channel RAW de-noise
0x5117	R_NOISELIST1_V_I	0x08	RW	Bit[7:0]: NoiseList1 for VS exposure channel RAW de-noise
0x5118	R_NOISELIST2_V_I	0x10	RW	Bit[7:0]: NoiseList2 for VS exposure channel RAW de-noise
0x5119	R_NOISELIST3_V_I	0x18	RW	Bit[7:0]: NoiseList3 for VS exposure channel RAW de-noise
0x511A	R_NOISELIST4_V_I	0x20	RW	Bit[7:0]: NoiseList4 for VS exposure channel RAW de-noise
0x511B	R_NOISELIST5_V_I	0x30	RW	Bit[7:0]: NoiseList5 for VS exposure channel RAW de-noise
0x511C	R_NOISELIST6_V_I	0x40	RW	Bit[7:0]: NoiseList6 for VS exposure channel RAW de-noise
0x511D	R_NOISELIST7_V_I	0x40	RW	Bit[7:0]: NoiseList7 for VS exposure channel RAW de-noise
0x511E	R_G_DNS_EN_V_I	0x00	RW	Bit[0]: Green channel de-noising for VS channel 0: Disable 1: Enable
0x511F	R_NOISE_YSLOP _V_I	0x04	RW	Bit[3:0]: Noise Y slop signal VS channel
0x5120	R_MAX_EDGE_THRE _V_I	0x3F	RW	Bit[7:0]: Maximum edge threshold VS channel

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4.5.3 UVDNS

UVDNS is designed to reduce UV noise. Besides the noise list, the two following parameters are used to increase the de-noise level in dark tone:

- shadow extra noise disable (0x5E88[5]): when set to 0, will increase de-noise level by register 0x5E88[4:0] in the dark tone
- shadow extra noise (0x5E88[4:0]): the extra amount will be added to the de-noise level in dark tone

table 4-13 UV_DNS control registers

address	register name	default value	R/W	description
0x5E80	R_NOISE_LIST_0	0x01	RW	Bit[4:0]: Noise list[0]
0x5E81	R_NOISE_LIST_1	0x02	RW	Bit[4:0]: Noise list[1]
0x5E82	R_NOISE_LIST_2	0x04	RW	Bit[4:0]: Noise list[2]
0x5E83	R_NOISE_LIST_3	0x08	RW	Bit[4:0]: Noise list[3]
0x5E84	R_NOISE_LIST_4	0x0C	RW	Bit[4:0]: Noise list[4]
0x5E85	R_NOISE_LIST_5	0x10	RW	Bit[4:0]: Noise list[5]
0x5E86	R_NOISE_LIST_6	0x14	RW	Bit[4:0]: Noise list[6]
0x5E87	R_NOISE_LIST_7	0x18	RW	Bit[4:0]: Noise list[7]
0x5E88	R_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x5E89	R_MANUAL_NOISE	0x0A	RW	Bit[4:0]: Manual noise
0x5E8A	RSVD	–	–	Reserved

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4.6 combine

The combine module will combine the L, S and VS channels to a single exposure channel with extended bit depth. It is enabled by default and can be disabled in register 0x5000[6].

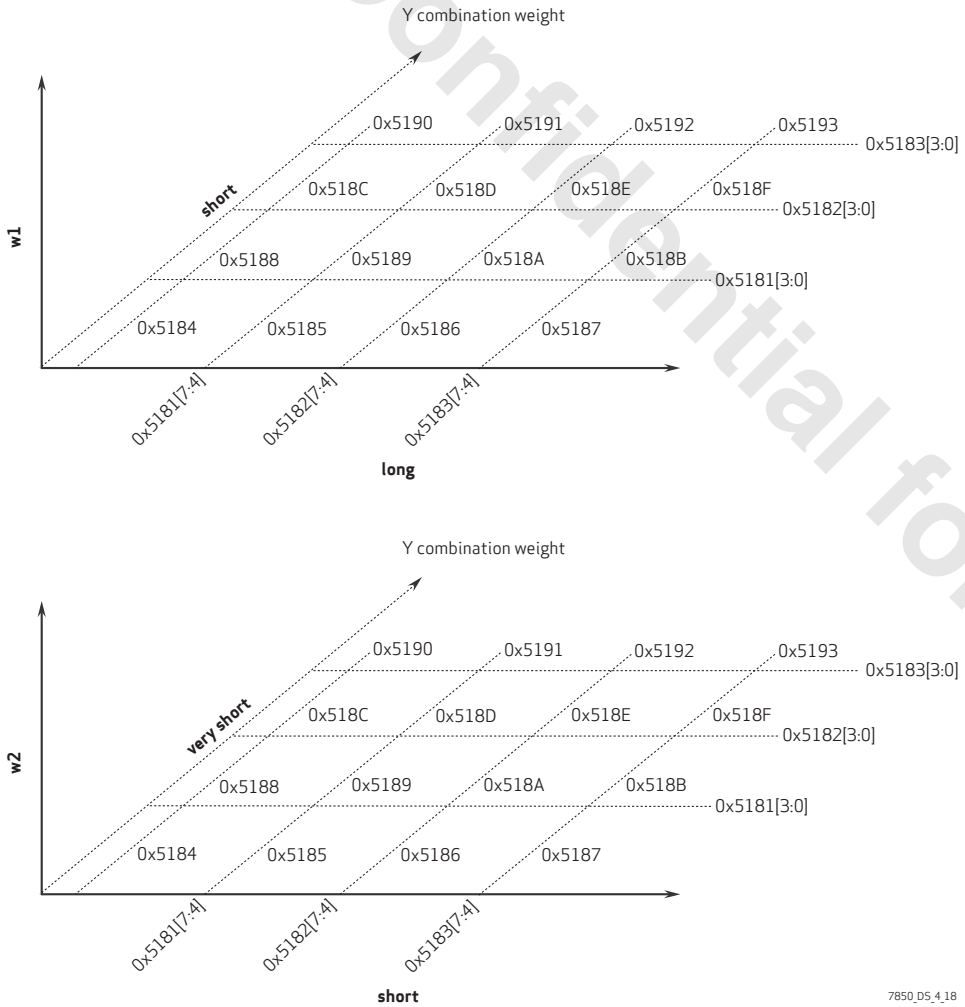
To prepare data for HDR processing, sensor RAW data is converted from Bayer pattern to RGBY format in a simple color interpolation procedure (simple CIP).

Y is calculated from BGR:

Y = (B+G×2+R)>>2

The combination result gives a combined weighted average of long, short and very short input.

figure 4-18 combine graph diagram



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Three exposure mode/ traffic exposure mode:

$D = D_L \times W_1 + D_S \times (1-W_1) \times W_2 + D_{VS} \times (1-W_1)(1-W_2)$

LS exposure mode:

$D = D_L \times W_1 + D_S \times (1-W_1)$

LVS exposure mode:

$D = D_L \times W_1 + D_{VS} \times (1-W_1)$

W_1 is the weight between L and S (VS in LVS exposure mode)

W_2 is the weight between S and VS (only available in three/ traffic exposure mode)

D denotes the exposure data

The weighting varies from pixel to pixel and W_1 and W_2 is interpolated from a look up table. The two channels with best SNR are combine for each pixel. So the combination is either between L and S, or S and VS.

In three/traffic exposure mode, there are four different combine mode (0x5180[1:0]):

0: HDRCombine, $D=D_L \times W_1 + D_S \times (1-W_1) \times W_2 + D_{VS} \times (1-W_1)(1-W_2)$

1: choose long, $D=D_L$, $W_1 = 1$, $W_2=0$

2: choose short, $D=D_S$, $W_1=0$, $W_2=1$

3: choose very short, $D=D_{VS}$, $W_1=0$, $W_2=0$

If traffic mode is enabled, there is a threshold {0x5197, 0x5198} to decide if the S channel pixel is a traffic light. When the S pixel brightness is higher than this threshold, it is defined as a traffic light and the threshold to modify the combine weights is given by registers 0x5199, 0x519A, 0x519B, and 0x519C.

In order to cancel QE difference between long and short pixel, a color matrix correction may be applied to S channel before combination 0x5180[3].

Suppose current RAW data is blue, then PreCMX will be:

$D' = M_{BB} \times B + M_{BG} \times G + M_{BR} \times R$

$D_{Snew} = D_S - B_S + D'$

The same process for green and red pixels of short exposure channel.

There is a number of parameters to adjust (see **table 4-15**) in the combine and tone mapping processing to get the best image quality for high dynamic range usage. Default values give a good overall HDR performance, but for special cases tuning can be done. Please contact your regional OmniVision FAE for assistance.

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table 4-14 combine_tonemap (sheet 1 of 3)

parameter	parameter function	register address	
		start	end
tone mapping enable	tone mapping enable 0: HDR data without tone mapping 1: tone mapped output	0x5001[0]	
shape smooth enable	smooth tone curve to avoid sharp angle or not	0x54A8	
combine work mode	combine work mode 00: use combination 01: use long exposure data as combine result 10: use short exposure data as combine result 11: use VS exposure data as combine result	0x5180	
compensate error enable	compensate inaccurate ratio between the exposure ratio and real data ratio	0x5180[2]	
auto tone mapping curve	use automatically generated tone curve	0x5408	
contrast enable	apply estimated contrast curve after local gamma implementation	0x5580[0]	
gain enhancement control	use gain to control contrast level	0x5406	
contrast boost	apply gamma gain between global and local gamma	0x5580[1]	
raw out bits	bit number for RAW HDR result	0x558A	
step E	combine error step between frames	0x5404	
combine threshold	combine thresholds	0x5181	0x5183
combine weight	combine weights	0x5184	0x5193
low and high contrast level	contrast level for high and low dynamic range	0x54B8	0x54B9
min and max dynamic range	dynamic range corresponding to low contrast level and high contrast level	0x540A	0x540B
curve step	curve change ratio step	0x5409	
YTh0~YTh3	threshold to modify weight between global and local gamma, when 0x5580[1]=1	0x5618	0x561F
manual tone curve	tone curve when auto tone mapping curve is not enabled (0xA5408=0)	0x546E	0x548D
light curve	lightest curve constraint for tone curve	0x542E	0x544D
dark curve	darkest curve constraint for tone curve	0x544E	0x546D
log target Y	normalized target for gamma estimation	0x54A2	0x54A7
gamma step	step (weight) between current mean and real target mean	0x54B2	
global gamma step	step between current gamma and estimated gamma	0x54AA	

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table 4-14 combine_tonemap (sheet 2 of 3)

parameter	parameter function	register address	
		start	end
min saturated level	minimum saturate level (int [0,255]) constraint	0x54A9	
final saturate threshold	maximum possible pixel number to be saturated for HDR gain applied	0x5194	0x5196
HDR gain step	HDR gain step	0x54AB	
global mean W	step between current mean and LogTarget to compute real target	0x54B1	
dynamic range list	dynamic range threshold to estimate gamma range	0x549A	0x549F
min gamma list	minimum gamma for different dynamic range	0x548E	0x5493
max gamma list	maximum gamma for different dynamic range	0x5494	0x5499
frame stable	frame stable is frame number of progressive preservation of saturated pixels	0x54B3	
local enhancement level	to preserve the saturated pixel number or not	0x54B4	
gamma comparison ratio	maximum ratio of local gamma compared to global gamma, base = 32	0x54B7	
TrafficSTh	S channel pixel is definitely not a traffic light, when S pixel brightness is less than this threshold	0x5197	
ThS	thresholds to modify combine weights if this pixel is possibly a traffic light	0x5199	
global mean stat ROI enable	true: direct statistic of global mean in ROI false: use windowed mean to calculate global mean	0x5580[4]	
global mean StatTh	minimum statistic pixel number to make ROI statistic effective	0x5594	0x5596
fish eye stat enable	true: for pixels in four corner windows, only inner triangle pixels are effective false: all pixels in corner windows are effective	0x5580[2]	
global gamma shift enable	true: using a global/preset gamma shift to estimated ones false: using estimated gamma only	0x54B5	
global gamma shift	additional gamma shift applied when GlobalGammaShiftEnable=true	0x54B6	
S prematrix enable	true: an additional matrix applied to S channel false: do not calibrate this pixel die matrix	55	
AutoCT enable	true: using AWB para to determine illuminant false: using D65 illuminant PreMatrix as default	0x54BB	
CTList0~CTList	thresholds of AWB para to determine illuminants	0x54C6	0x54CB

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table 4-14 combine_tonemap (sheet 3 of 3)

parameter	parameter function	register address	
		start	end
InvMLMS_D_	matrix pre-applied to S channel for D65	0x54CC	0x54DD
InvMLMS_A_	matrix pre-applied to S channel for A	0x54F0	0x5501
InvMLMS_C_	matrix pre-applied to S channel for CWF	0x54DE	0x54EF

table 4-15 combine control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5180	R_COMBINE_CTRL	0x0C	RW	Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: Use combination 01: Use long exposure data as combine result 10: Use short exposure data as combine result 11: Use very short exposure data as combine result
0x5181	R_COMBINE_THRE_0	0x95	RW	Combine Threshold 0 Bit[7:4]: Long Bit[3:0]: Short
0x5182	R_COMBINE_THRE_1	0xA8	RW	Combine Threshold 1 Bit[7:4]: Long Bit[3:0]: Short
0x5183	R_COMBINE_THRE_2	0xAA	RW	Combine Threshold 2 Bit[7:4]: Long Bit[3:0]: Short
0x5184	R_COMBINE_WEIGHT_0_0	0x80	RW	Bit[7:0]: Combine weight 0,0
0x5185	R_COMBINE_WEIGHT_0_1	0x80	RW	Bit[7:0]: Combine weight 0,1
0x5186	R_COMBINE_WEIGHT_0_2	0x60	RW	Bit[7:0]: Combine weight 0,2
0x5187	R_COMBINE_WEIGHT_0_3	0x40	RW	Bit[7:0]: Combine weight 0,3
0x5188	R_COMBINE_WEIGHT_1_0	0x80	RW	Bit[7:0]: Combine weight 1,0
0x5189	R_COMBINE_WEIGHT_1_1	0x80	RW	Bit[7:0]: Combine weight 1,1
0x518A	R_COMBINE_WEIGHT_1_2	0x40	RW	Bit[7:0]: Combine weight 1,2
0x518B	R_COMBINE_WEIGHT_1_3	0x20	RW	Bit[7:0]: Combine weight 1,3
0x518C	R_COMBINE_WEIGHT_2_0	0x80	RW	Bit[7:0]: Combine weight 2,0

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table 4-15 combine control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x518D	R_COMBINE_WEIGHT_2_1	0x80	RW	Bit[7:0]: Combine weight 2,1
0X518E	R_COMBINE_WEIGHT_2_2	0x20	RW	Bit[7:0]: Combine weight 2,2
0x518F	R_COMBINE_WEIGHT_2_3	0x00	RW	Bit[7:0]: Combine weight 2,3
0x5190	R_COMBINE_WEIGHT_3_0	0x80	RW	Bit[7:0]: Combine weight 3,0
0x5191	R_COMBINE_WEIGHT_3_1	0x80	RW	Bit[7:0]: Combine weight 3,1
0x5192	R_COMBINE_WEIGHT_3_2	0x00	RW	Bit[7:0]: Combine weight 3,2
0x5193	R_COMBINE_WEIGHT_3_3	0x00	RW	Bit[7:0]: Combine weight 3,3
0x5194	R_SATURATE_THRE_B2	0x00	RW	Bit[2:0]: Final saturate threshold[18:16]
0x5195	R_SATURATE_THRE_B1	0x00	RW	Bit[7:0]: Final saturate threshold[15:8]
0x5196	R_SATURATE_THRE_B0	0x20	RW	Bit[7:0]: Final saturate threshold[7:0]
0x5197	R_TRAFFIC_S_TH_H	0x28	RW	Bit[7:0]: Traffic S threshold[15:8]
0x5198	R_TRAFFIC_S_TH_L	0x00	RW	Bit[7:0]: Traffic S threshold[7:0]
0x5199	R_TH_S_0_H	0x08	RW	Bit[7:0]: m_nThS[0][15:8]
0x519A	R_TH_S_0_L	0x00	RW	Bit[7:0]: m_nThS[0[7:0]
0x519B	R_TH_S_1_H	0x10	RW	Bit[7:0]: m_nThS[1][15:8]
0x519C	R_TH_S_1_L	0x00	RW	Bit[7:0]: m_nThS[1][7:0]
0x519D	R_THS_DINV	0x20	RW	Bit[7:0]: m_nThSDinv, equal to (2^16)/(m_nThS[1]-m_nThS[0])
0x51A0~ 0x51F8	RSVD	–	–	Reserved

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4.7 tone mapping

Tone mapping gets data from combine and is used to map the data to a specified bit-width in order to approximate the appearance of high dynamic range images. The output bit-width can be 16 bits, 18 bits, or 20 bits.

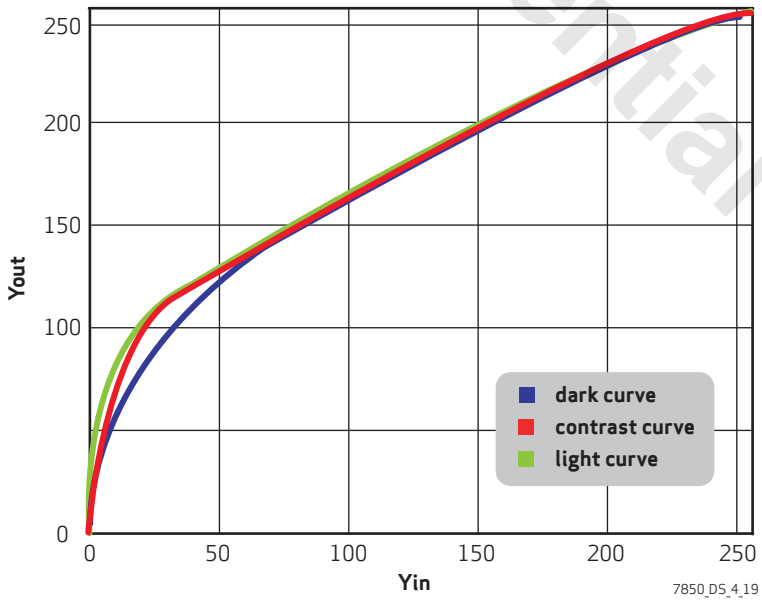
The OV7850 must be configured to RAW output mode first, then register 0x3024[6:4] must be set to select output bit-width. The output bit-width can be manually set in register 0x558A[5] and then register 0x558A[4:0] can be set to any value from 10 to 20. For RAW10 output format, tone mapping is disabled.

There are two steps in tone mapping procedure:

- global and local tone mapping where gamma is applied on luminance channel and keeps chrominance unchanged, so it solely compresses the data bit depth
- contrast adjustment to equalize histogram for better HDR rendering

The 16-bin histogram is achieved from the local tone mapped image. The standard HE mapping curve is weighted by a linear (45-degree) curve using a parameter called ContrastLevel. The contrast level is typically adjusted by dynamic range and camera gain. The greater the dynamic range is, the greater the possible contrast level. Because high gain usually introduces high noise which will also be amplified in contrast enhancement, the contrast level will be kept to a low level if the gain is high. After this curve estimation is done, tone curve is restricted between two curves (i.e., the dark and light curves to avoid over-enhancement). The contrast curve, light curve and dark curve are shown in **figure 4-19**.

figure 4-19 tone curve



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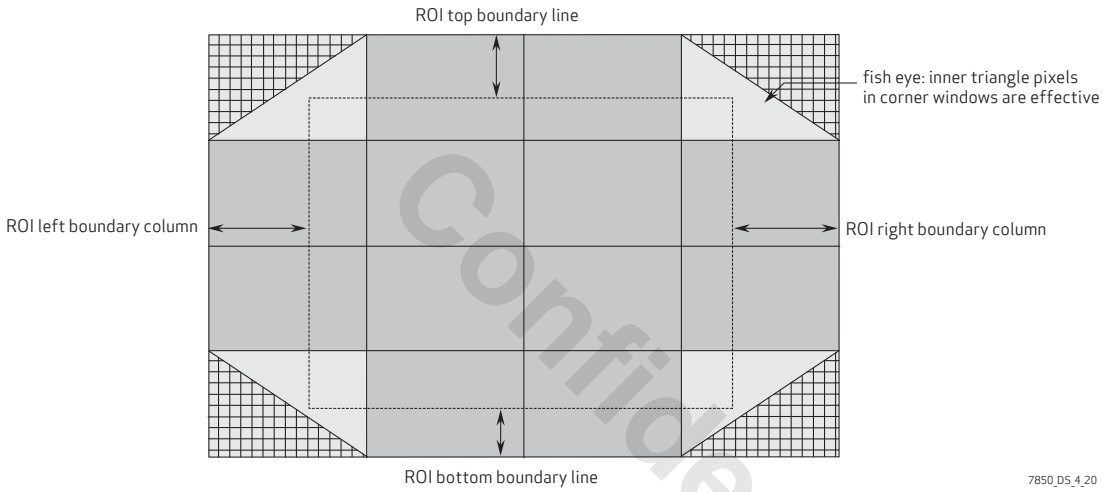
The local tone mapping procedure splits the input image into a 4x4 fixed array. The gamma gain calculation is based on the 4x4 window and then applied to image data. Local mean is calculated as the average value for each window. If fish eye statistics is enabled by setting register 0x5580[2] to 1, special statistics are done for the four corner windows. If fish eye statistics is disabled, the statistics will be the same for each window.

figure 4-20 tone mapping statistics diagram



Global tone mapping supports ROI and the ROI is set in registers 0x558C~0x5593. For different ROI control options, see register 0x5580[7:4].

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table 4-16 tone mapping registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580	TONE_MAPPING_CTRL0	0x03	RW	Bit[7:5]: global_mean_sh ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical direction 010: 1/16 sample in both horizontal and vertical direction 011: 1/64 sample in both horizontal and vertical direction 100: 1/256 sample in both horizontal and vertical direction Others: Not supported Bit[4]: global_mean_roi_en 0: Global mean is calculated from local mean by getting average value of 4x4 window local mean 1: Global mean is calculated from selected ROI Bit[3]: hdr_gain_sh_en 0: Use log value directly from combine output 1: Add a shift value to compensate combine output log value Bit[2]: Enable fish eye statistics 0: All pixels in corner windows are effective 1: For pixels in four corner windows, only inner triangle pixels are effective Bit[1]: Contrast boost enable Bit[0]: Contrast enable
0x5581~ 0x5589	RSVD	–	–	Reserved
0x558A	TONE_MAPPING_CTRL2	0x0A	RW	Bit[5]: Enable manual output bit-width 0: Use auto raw_out_bit value from input port 1: Use manual raw_out_bit value from internal register Bit[4:0]: raw_out_bit

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table 4-16 tone mapping registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x558B	RSVD	–	–	Reserved
0x558C	ROI_TOP_BYTE1	0x00	RW	Bit[1:0]: ROI top boundary line[9:8]
0x558D	ROI_TOP_BYTE0	0x10	RW	Bit[7:0]: ROI top boundary line[7:0]
0x558E	ROI_BOTTOM_BYTE1	0x00	RW	Bit[1:0]: ROI bottom boundary line[9:8]
0x558F	ROI_BOTTOM_BYTE0	0x10	RW	Bit[7:0]: ROI bottom boundary line[7:0]
0x5590	ROI_LEFT_BYTE1	0x00	RW	Bit[1:0]: ROI left boundary column[9:8]
0x5591	ROI_LEFT_BYTE0	0x10	RW	Bit[7:0]: ROI left boundary column[7:0]
0x5592	ROI_RIGHT_BYTE1	0x00	RW	Bit[1:0]: ROI right boundary column[9:8]
0x5593	ROI_RIGHT_BYTE0	0x10	RW	Bit[7:0]: ROI right boundary column[7:0]
0x5594	GLOBAL_ST_TH_BYTE2	0x00	RW	Bit[3:0]: Global mean statistic threshold[19:16]
0x5595	GLOBAL_ST_TH_BYTE1	0x04	RW	Bit[7:0]: Global mean statistic threshold[15:8]
0x5596	GLOBAL_ST_TH_BYTE0	0x00	RW	Bit[7:0]: Global mean statistic threshold[7:0]
0x5597	HDR_GAIN_SH_BYTE1	0x00	RW	Bit[4:0]: Log HDR gain shift[12:8]
0x5598	HDR_GAIN_SH_BYTE0	0x00	RW	Bit[7:0]: Log HDR gain shift[7:0]
0x5599~ 0x5617	RSVD	–	–	Reserved
0x5618	Y_TH0_BYTE1	0x00	RW	Bit[7:0]: Y threshold 0[15:8]
0x5619	Y_TH0_BYTE0	0x00	RW	Bit[7:0]: Y threshold 0[7:0]
0x561A	Y_TH1_BYTE1	0x00	RW	Bit[7:0]: Y threshold 1[15:8]
0x561B	Y_TH1_BYTE0	0x00	RW	Bit[7:0]: Y threshold 1[7:0]
0x561C	Y_TH2_BYTE1	0x00	RW	Bit[7:0]: Y threshold 2[15:8]
0x561D	Y_TH2_BYTE0	0x00	RW	Bit[7:0]: Y threshold 2[7:0]
0x561E	Y_TH3_BYTE1	0x00	RW	Bit[7:0]: Y threshold 3[15:8]
0x561F	Y_TH3_BYTE0	0x00	RW	Bit[7:0]: Y threshold 3[7:0]
0x5621~ 0x56A7	RSVD	–	–	Reserved

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A gain is applied to boost the dark area of a high dynamic range scene. Boost gain is dependent on register 0x54B7. If register 0x54B7's value is 0x20, that means no boost gain. Gain is not applied to all pixels, only pixels falling in a luminance range will be boosted. The register range is 0x54BE~0x54C5.

brightness = 256/(2^(20 - register value/0x800))

The image is divided to 4x4 blocks and the gain of each pixel is interpolated from the neighboring grids.

figure 4-21 local tone mapping diagram

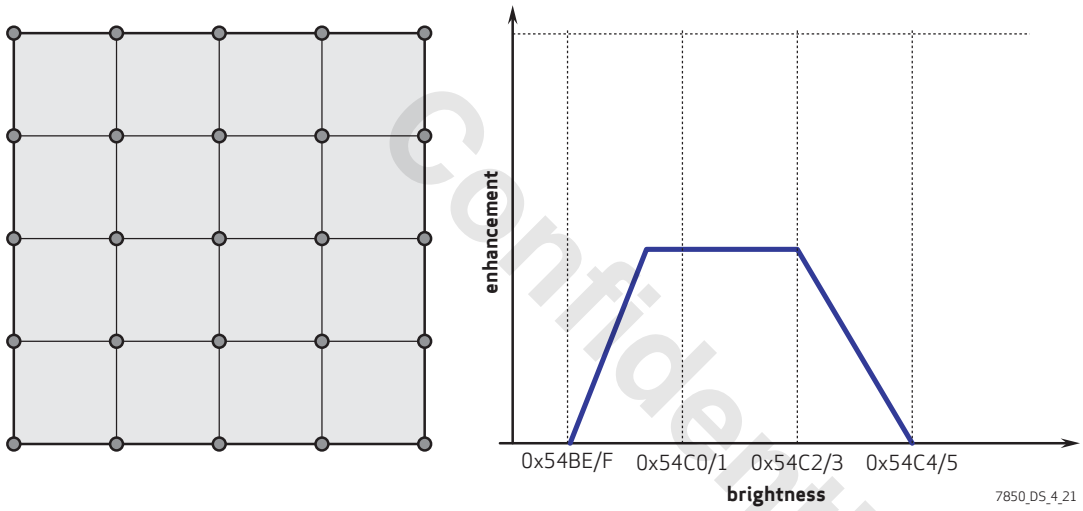

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table 4-17 HDR control registers (sheet 1 of 15)

address	register name	default value	R/W	description
0x5400	COMBINEERRORCONTROL POINT_BYTE0	–	–	Bit[7:0]: Threshold to enable combination error statistics calculation[7:0]
0x5401	COMBINEERRORCONTROL POINT_BYTE1	–	–	Bit[7:0]: Threshold to enable combination error statistics calculation[15:8]
0x5402	COMBINEERRORCONTROL POINT_BYTE2	–	–	Bit[7:0]: Threshold to enable combination error statistics calculation[23:16]
0x5403	COMBINEERRORCONTROL POINT_BYTE3	–	–	Bit[7:0]: Threshold to enable combination error statistics calculation[31:24]
0x5404	STEPE	–	–	Combine Error Change Step

table 4-17 HDR control registers (sheet 2 of 15)

address	register name	default value	R/W	description
0x5405	TONEMAPPINGENABLE	–	–	Tone Mapping Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5406	GAINENHANCEMENT CONTROL	–	–	Auto Tone Curve Enhancement Level Reduction Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5407	MANUALGAMMAENABLE	–	–	Manual Tone Compression Gamma Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5408	AUTOTONEMAPPINGCURVE	–	–	Auto Tone Mapping Curve Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5409	CURVESTEP	–	–	Tone Curve Change Step
0x540A	MINDYNAMICRANGE_H	–	–	Bit[7:0]: Low bound of dynamic range for tone curve reduction[15:8]
0x540B	MINDYNAMICRANGE_L	–	–	Bit[7:0]: Low bound of dynamic range for tone curve reduction[7:0]
0x540C	MAXDYNAMICRANGE_H	–	–	Bit[7:0]: High bound of dynamic range for tone curve reduction[15:8]
0x540D	MAXDYNAMICRANGE_L	–	–	Bit[7:0]: High bound of dynamic range for tone curve reduction[7:0]

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table 4-17 HDR control registers (sheet 3 of 15)

address	register name	default value	R/W	description
0x540E	GAMMALIST_0_H	–	–	Bit[7:0]: Base curve for tone curve P0[15:8]
0x540F	GAMMALIST_0_L	–	–	Bit[7:0]: Base curve for tone curve P0[7:0]
0x5410	GAMMALIST_1_H	–	–	Bit[7:0]: Base curve for tone curve P1[15:8]
0x5411	GAMMALIST_1_L	–	–	Bit[7:0]: Base curve for tone curve P1[7:0]
0x5412	GAMMALIST_2_H	–	–	Bit[7:0]: Base curve for tone curve P2[15:8]
0x5413	GAMMALIST_2_L	–	–	Bit[7:0]: Base curve for tone curve P2[7:0]
0x5414	GAMMALIST_3_H	–	–	Bit[7:0]: Base curve for tone curve P3[15:8]
0x5415	GAMMALIST_3_L	–	–	Bit[7:0]: Base curve for tone curve P3[7:0]
0x5416	GAMMALIST_4_H	–	–	Bit[7:0]: Base curve for tone curve P4[15:8]
0x5417	GAMMALIST_4_L	–	–	Bit[7:0]: Base curve for tone curve P4[7:0]
0x5418	GAMMALIST_5_H	–	–	Bit[7:0]: Base curve for tone curve P5[15:8]
0x5419	GAMMALIST_5_L	–	–	Bit[7:0]: Base curve for tone curve P5[7:0]
0x541A	GAMMALIST_6_H	–	–	Bit[7:0]: Base curve for tone curve P6[15:8]
0x541B	GAMMALIST_6_L	–	–	Bit[7:0]: Base curve for tone curve P6[7:0]
0x541C	GAMMALIST_7_H	–	–	Bit[7:0]: Base curve for tone curve P7[15:8]
0x541D	GAMMALIST_7_L	–	–	Bit[7:0]: Base curve for tone curve P7[7:0]
0x541E	GAMMALIST_8_H	–	–	Bit[7:0]: Base curve for tone curve P8[15:8]
0x541F	GAMMALIST_8_L	–	–	Bit[7:0]: Base curve for tone curve P8[7:0]
0x5420	GAMMALIST_9_H	–	–	Bit[7:0]: Base curve for tone curve P9[15:8]

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table 4-17 HDR control registers (sheet 4 of 15)

address	register name	default value	R/W	description
0x5421	GAMMALIST_9_L	–	–	Bit[7:0]: Base curve for tone curve P9[7:0]
0x5422	GAMMALIST_10_H	–	–	Bit[7:0]: Base curve for tone curve P10[15:8]
0x5423	GAMMALIST_10_L	–	–	Bit[7:0]: Base curve for tone curve P10[7:0]
0x5424	GAMMALIST_11_H	–	–	Bit[7:0]: Base curve for tone curve P11[15:8]
0x5425	GAMMALIST_11_L	–	–	Bit[7:0]: Base curve for tone curve P11[7:0]
0x5426	GAMMALIST_12_H	–	–	Bit[7:0]: Base curve for tone curve P12[15:8]
0x5427	GAMMALIST_12_L	–	–	Bit[7:0]: Base curve for tone curve P12[7:0]
0x5428	GAMMALIST_13_H	–	–	Bit[7:0]: Base curve for tone curve P13[15:8]
0x5429	GAMMALIST_13_L	–	–	Bit[7:0]: Base curve for tone curve P13[7:0]
0x542A	GAMMALIST_14_H	–	–	Bit[7:0]: Base curve for tone curve P14[15:8]
0x542B	GAMMALIST_14_L	–	–	Bit[7:0]: Base curve for tone curve P14[7:0]
0x542C	GAMMALIST_15_H	–	–	Bit[7:0]: Base curve for tone curve P15[15:8]
0x542D	GAMMALIST_15_L	–	–	Bit[7:0]: Base curve for tone curve P15[7:0]
0x542E	LIGHTCURVE_0_H	–	–	Bit[7:0]: High bound of tone curve P0[15:8]
0x542F	LIGHTCURVE_0_L	–	–	Bit[7:0]: High bound of tone curve P0[7:0]
0x5430	LIGHTCURVE_1_H	–	–	Bit[7:0]: High bound of tone curve P1[15:8]
0x5431	LIGHTCURVE_1_L	–	–	Bit[7:0]: High bound of tone curve P1[7:0]
0x5432	LIGHTCURVE_2_H	–	–	Bit[7:0]: High bound of tone curve P2[15:8]
0x5433	LIGHTCURVE_2_L	–	–	Bit[7:0]: High bound of tone curve P2[7:0]

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table 4-17 HDR control registers (sheet 5 of 15)

address	register name	default value	R/W	description
0x5434	LIGHTCURVE_3_H	–	–	Bit[7:0]: High bound of tone curve P3[15:8]
0x5435	LIGHTCURVE_3_L	–	–	Bit[7:0]: High bound of tone curve P3[7:0]
0x5436	LIGHTCURVE_4_H	–	–	Bit[7:0]: High bound of tone curve P4[15:8]
0x5437	LIGHTCURVE_4_L	–	–	Bit[7:0]: High bound of tone curve P4[7:0]
0x5438	LIGHTCURVE_5_H	–	–	Bit[7:0]: High bound of tone curve P5[15:8]
0x5439	LIGHTCURVE_5_L	–	–	Bit[7:0]: High bound of tone curve P5[7:0]
0x543A	LIGHTCURVE_6_H	–	–	Bit[7:0]: High bound of tone curve P6[15:8]
0x543B	LIGHTCURVE_6_L	–	–	Bit[7:0]: High bound of tone curve P6[7:0]
0x543C	LIGHTCURVE_7_H	–	–	Bit[7:0]: High bound of tone curve P7[15:8]
0x543D	LIGHTCURVE_7_L	–	–	Bit[7:0]: High bound of tone curve P7[7:0]
0x543E	LIGHTCURVE_8_H	–	–	Bit[7:0]: High bound of tone curve P8[15:8]
0x543F	LIGHTCURVE_8_L	–	–	Bit[7:0]: High bound of tone curve P8[7:0]
0x5440	LIGHTCURVE_9_H	–	–	Bit[7:0]: High bound of tone curve P9[15:8]
0x5441	LIGHTCURVE_9_L	–	–	Bit[7:0]: High bound of tone curve P9[7:0]
0x5442	LIGHTCURVE_10_H	–	–	Bit[7:0]: High bound of tone curve P10[15:8]
0x5443	LIGHTCURVE_10_L	–	–	Bit[7:0]: High bound of tone curve P10[7:0]
0x5444	LIGHTCURVE_11_H	–	–	Bit[7:0]: High bound of tone curve P11[15:8]
0x5445	LIGHTCURVE_11_L	–	–	Bit[7:0]: High bound of tone curve P11[7:0]
0x5446	LIGHTCURVE_12_H	–	–	Bit[7:0]: High bound of tone curve P12[15:8]

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address	register name	default value	R/W	description
0x5447	LIGHTCURVE_12_L	–	–	Bit[7:0]: High bound of tone curve P12[7:0]
0x5448	LIGHTCURVE_13_H	–	–	Bit[7:0]: High bound of tone curve P13[15:8]
0x5449	LIGHTCURVE_13_L	–	–	Bit[7:0]: High bound of tone curve P13[7:0]
0x544A	LIGHTCURVE_14_H	–	–	Bit[7:0]: High bound of tone curve P14[15:8]
0x544B	LIGHTCURVE_14_L	–	–	Bit[7:0]: High bound of tone curve P14[7:0]
0x544C	LIGHTCURVE_15_H	–	–	Bit[7:0]: High bound of tone curve P15[15:8]
0x544D	LIGHTCURVE_15_L	–	–	Bit[7:0]: High bound of tone curve P15[7:0]
0x544E	DARKCURVE_0_H	–	–	Bit[7:0]: Low bound of tone curve P0[15:8]
0x544F	DARKCURVE_0_L	–	–	Bit[7:0]: Low bound of tone curve P0[7:0]
0x5450	DARKCURVE_1_H	–	–	Bit[7:0]: Low bound of tone curve P1[15:8]
0x5451	DARKCURVE_1_L	–	–	Bit[7:0]: Low bound of tone curve P1[7:0]
0x5452	DARKCURVE_2_H	–	–	Bit[7:0]: Low bound of tone curve P2[15:8]
0x5453	DARKCURVE_2_L	–	–	Bit[7:0]: Low bound of tone curve P2[7:0]
0x5454	DARKCURVE_3_H	–	–	Bit[7:0]: Low bound of tone curve P3[15:8]
0x5455	DARKCURVE_3_L	–	–	Bit[7:0]: Low bound of tone curve P3[7:0]
0x5456	DARKCURVE_4_H	–	–	Bit[7:0]: Low bound of tone curve P4[15:8]
0x5457	DARKCURVE_4_L	–	–	Bit[7:0]: Low bound of tone curve P4[7:0]
0x5458	DARKCURVE_5_H	–	–	Bit[7:0]: Low bound of tone curve P5[15:8]
0x5459	DarkCurve_5_l	–	–	Bit[7:0]: Low bound of tone curve P5[7:0]

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address	register name	default value	R/W	description
0x545A	DARKCURVE_6_H	–	–	Bit[7:0]: Low bound of tone curve P6[15:8]
0x545B	DARKCURVE_6_L	–	–	Bit[7:0]: Low bound of tone curve P6[7:0]
0x545C	DARKCURVE_7_H	–	–	Bit[7:0]: Low bound of tone curve P7[15:8]
0x545D	DARKCURVE_7_L	–	–	Bit[7:0]: Low bound of tone curve P7[7:0]
0x545E	DARKCURVE_8_H	–	–	Bit[7:0]: Low bound of tone curve P8[15:8]
0x545F	DARKCURVE_8_L	–	–	Bit[7:0]: Low bound of tone curve P8[7:0]
0x5460	DARKCURVE_9_H	–	–	Bit[7:0]: Low bound of tone curve P9[15:8]
0x5461	DARKCURVE_9_L	–	–	Bit[7:0]: Low bound of tone curve P9[7:0]
0x5462	DARKCURVE_10_H	–	–	Bit[7:0]: Low bound of tone curve P10[15:8]
0x5463	DARKCURVE_10_L	–	–	Bit[7:0]: Low bound of tone curve P10[7:0]
0x5464	DARKCURVE_11_H	–	–	Bit[7:0]: Low bound of tone curve P11[15:8]
0x5465	DARKCURVE_11_L	–	–	Bit[7:0]: Low bound of tone curve P11[7:0]
0x5466	DARKCURVE_12_H	–	–	Bit[7:0]: Low bound of tone curve P12[15:8]
0x5467	DARKCURVE_12_L	–	–	Bit[7:0]: Low bound of tone curve P12[7:0]
0x5468	DARKCURVE_13_H	–	–	Bit[7:0]: Low bound of tone curve P13[15:8]
0x5469	DARKCURVE_13_L	–	–	Bit[7:0]: Low bound of tone curve P13[7:0]
0x546A	DARKCURVE_14_H	–	–	Bit[7:0]: Low bound of tone curve P14[15:8]
0x546B	DARKCURVE_14_L	–	–	Bit[7:0]: Low bound of tone curve P14[7:0]
0x546C	DARKCURVE_15_H	–	–	Bit[7:0]: Low bound of tone curve P15[15:8]

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address	register name	default value	R/W	description
0x546D	DARKCURVE_15_L	–	–	Bit[7:0]: Low bound of tone curve P15[7:0]
0x546E	MANUALTONECURVE_0_H	–	–	Bit[7:0]: Manual tone curve P0[15:8]
0x546F	MANUALTONECURVE_0_L	–	–	Bit[7:0]: Manual tone curve P0[7:0]
0x5470	MANUALTONECURVE_1_H	–	–	Bit[7:0]: Manual tone curve P1[15:8]
0x5471	MANUALTONECURVE_1_L	–	–	Bit[7:0]: Manual tone curve P1[7:0]
0x5472	MANUALTONECURVE_2_H	–	–	Bit[7:0]: Manual tone curve P2[15:8]
0x5473	MANUALTONECURVE_2_L	–	–	Bit[7:0]: Manual tone curve P2[7:0]
0x5474	MANUALTONECURVE_3_H	–	–	Bit[7:0]: Manual tone curve P3[15:8]
0x5475	MANUALTONECURVE_3_L	–	–	Bit[7:0]: Manual tone curve P3[7:0]
0x5476	MANUALTONECURVE_4_H	–	–	Bit[7:0]: Manual tone curve P4[15:8]
0x5477	MANUALTONECURVE_4_L	–	–	Bit[7:0]: Manual tone curve P4[7:0]
0x5478	MANUALTONECURVE_5_H	–	–	Bit[7:0]: Manual tone curve P5[15:8]
0x5479	MANUALTONECURVE_5_L	–	–	Bit[7:0]: Manual tone curve P5[7:0]
0x547A	MANUALTONECURVE_6_H	–	–	Bit[7:0]: Manual tone curve P6[15:8]
0x547B	MANUALTONECURVE_6_L	–	–	Bit[7:0]: Manual tone curve P6[7:0]
0x547C	MANUALTONECURVE_7_H	–	–	Bit[7:0]: Manual tone curve P7[15:8]
0x547D	MANUALTONECURVE_7_L	–	–	Bit[7:0]: Manual tone curve P7[7:0]
0x547E	MANUALTONECURVE_8_H	–	–	Bit[7:0]: Manual tone curve P8[15:8]
0x547F	MANUALTONECURVE_8_L	–	–	Bit[7:0]: Manual tone curve P8[7:0]
0x5480	MANUALTONECURVE_9_H	–	–	Bit[7:0]: Manual tone curve P9[15:8]
0x5481	MANUALTONECURVE_9_L	–	–	Bit[7:0]: Manual tone curve P9[7:0]
0x5482	MANUALTONECURVE_10_H	–	–	Bit[7:0]: Manual tone curve P10[15:8]
0x5483	MANUALTONECURVE_10_L	–	–	Bit[7:0]: Manual tone curve P10[7:0]
0x5484	MANUALTONECURVE_11_H	–	–	Bit[7:0]: Manual tone curve P11[15:8]
0x5485	MANUALTONECURVE_11_L	–	–	Bit[7:0]: Manual tone curve P11[7:0]
0x5486	MANUALTONECURVE_12_H	–	–	Bit[7:0]: Manual tone curve P12[15:8]
0x5487	MANUALTONECURVE_12_L	–	–	Bit[7:0]: Manual tone curve P12[7:0]
0x5488	MANUALTONECURVE_13_H	–	–	Bit[7:0]: Manual tone curve P13[15:8]
0x5489	MANUALTONECURVE_13_L	–	–	Bit[7:0]: Manual tone curve P13[7:0]

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address	register name	default value	R/W	description
0x548A	MANUALTONECURVE_14_H	–	–	Bit[7:0]: Manual tone curve P14[15:8]
0x548B	MANUALTONECURVE_14_L	–	–	Bit[7:0]: Manual tone curve P14[7:0]
0x548C	MANUALTONECURVE_15_H	–	–	Bit[7:0]: Manual tone curve P15[15:8]
0x548D	MANUALTONECURVE_15_L	–	–	Bit[7:0]: Manual tone curve P15[7:0]
0x548E	MINGAMMALIST_0_H	–	–	Bit[7:0]: Min tone compression gamma list 1[15:8]
0x548F	MINGAMMALIST_0_L	–	–	Bit[7:0]: Min tone compression gamma list 1[7:0]
0x5490	MINGAMMALIST_1_H	–	–	Bit[7:0]: Min tone compression gamma list 2[15:8]
0x5491	MINGAMMALIST_1_L	–	–	Bit[7:0]: Min tone compression gamma list 2[7:0]
0x5492	MINGAMMALIST_2_H	–	–	Bit[7:0]: Min tone compression gamma list 3[15:8]
0x5493	MINGAMMALIST_2_L	–	–	Bit[7:0]: Min tone compression gamma list 3[7:0]
0x5494	MAXGAMMALIST_0_H	–	–	Bit[7:0]: Max tone compression gamma list 1[15:8]
0x5495	MAXGAMMALIST_0_L	–	–	Bit[7:0]: Max tone compression gamma list 1[7:0]
0x5496	MAXGAMMALIST_1_H	–	–	Bit[7:0]: Max tone compression gamma list 2[15:8]
0x5497	MAXGAMMALIST_1_L	–	–	Bit[7:0]: Max tone compression gamma list 2[7:0]
0x5498	MAXGAMMALIST_2_H	–	–	Bit[7:0]: Max tone compression gamma list 3[15:8]
0x5499	MAXGAMMALIST_2_L	–	–	Bit[7:0]: Max tone compression gamma list 3[7:0]
0x549A	DYNAMICRANGELIST_0_H	–	–	Bit[7:0]: Dynamic range list 1[15:8]
0x549B	DYNAMICRANGELIST_0_L	–	–	Bit[7:0]: Dynamic range list 1[7:0]
0x549C	DYNAMICRANGELIST_1_H	–	–	Bit[7:0]: Dynamic range list 2[15:8]
0x549D	DYNAMICRANGELIST_1_L	–	–	Bit[7:0]: Dynamic range list 2[7:0]
0x549E	DYNAMICRANGELIST_2_H	–	–	Bit[7:0]: Dynamic range list 3[15:8]
0x549F	DYNAMICRANGELIST_2_L	–	–	Bit[7:0]: Dynamic range list 3[7:0]

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address	register name	default value	R/W	description
0x54A0	MANUALGAMMA_H	–	–	Bit[7:0]: Manual tone compression gamma[15:8]
0x54A1	MANUALGAMMA_L	–	–	Bit[7:0]: Manual tone compression gamma[7:0]
0x54A2	LOGTARGETY_0_H	–	–	Bit[7:0]: Image mean value target for frame A in ABC mode[15:8]
0x54A3	LOGTARGETY_0_L	–	–	Bit[7:0]: Image mean value target for frame A in ABC mode[7:0]
0x54A4	LOGTARGETY_1_H	–	–	Bit[7:0]: Image mean value target for frame B in ABC mode[15:8]
0x54A5	LOGTARGETY_1_L	–	–	Bit[7:0]: Image mean value target for frame B in ABC mode[7:0]
0x54A6	LOGTARGETY_2_H	–	–	Bit[7:0]: Image mean value target for frame C in ABC mode[15:8]
0x54A7	LOGTARGETY_2_L	–	–	Bit[7:0]: Image mean value target for frame C in ABC mode[7:0]
0x54A8	SHAPESMOOTHENABLE	–	–	Tone Curve Smooth Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x54A9	MINSATURATELEVEL	–	–	Minimum Saturate Level for VS/Short
0x54AA	GLOBALGAMMASTEP	–	–	Tone Compression Gamma Step
0x54AB	HDRGAINSTEP	–	–	HDR Gain Step
0x54AC	REDUCENOISEINDARK ENABLE	–	–	Reduce Noise for Dark Scenes Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x54AD	REDUCENOISEMINGAIN	–	–	Low Gain Boundary for Reduce Noise Function
0x54AE	REDUCENOISEMAXGAIN_H	–	–	Bit[7:0]: High gain boundary for reduce noise function[15:8]

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address	register name	default value	R/W	description
0x54AF	REDUCENOISEMAXGAIN_L	–	–	Bit[7:0]: High gain boundary for reduce noise function[7:0]
0x54B0	REDUCENOISESTEP	–	–	Gain Step Value for Reduce Noise
0x54B1	GLOBALMEANW	–	–	Current Global Mean Value Weight to Final Target
0x54B2	GAMMASTEP	–	–	Tone Compression Gamma Change Step
0x54B3	FRAMESTABLE	–	–	Frame Stable Number for Saturated Pixel Preserved Mode (2^framestable)
0x54B4	SATURATEDPIXELP RESERVED	–	–	Saturated Pixel Preserved Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x54B5	GLOBALGAMMASHIFT ENABLE	–	–	Tone Compression Gamma Shift Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x54B6	GLOBALGAMMASHIFT	–	–	Tone Compression Gamma Shift Value
0x54B7	LOCALENHANCEMENT LEVEL	–	–	Local Enhancement Level
0x54B8	LOWCONTRASTLEVEL	–	–	Tone Curve Enhancement Low Level
0x54B9	HIGHCONTRASTLEVEL	–	–	Tone Curve Enhancement High Level
0x54BB	SPREAUTOCTENABLE	–	–	SPD Pre Matrix Illuminant Adaptation Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x54BC	EXPCHANGELOGTH_H	–	–	Bit[7:0]: Exposure change threshold[15:8]

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address	register name	default value	R/W	description
0x54BD	EXPCHANGELOGTH_L	–	–	Bit[7:0]: Exposure change threshold[7:0]
0x54BE	YTH0TARGET_0_H	–	–	Bit[7:0]: Dark contrast enhancement Y Th0[15:8]
0x54BF	YTH0TARGET_0_L	–	–	Bit[7:0]: Dark contrast enhancement Y Th0[7:0]
0x54C0	YTH1TARGET_1_H	–	–	Bit[7:0]: Dark contrast enhancement Y Th1[15:8]
0x54C1	YTH1TARGET_1_L	–	–	Bit[7:0]: Dark contrast enhancement Y Th1[7:0]
0x54C2	YTH0TARGET_2_H	–	–	Bit[7:0]: Dark contrast enhancement Y Th2[15:8]
0x54C3	YTH0TARGET_2_L	–	–	Bit[7:0]: Dark contrast enhancement Y Th2[7:0]
0x54C4	YTH1TARGET_3_H	–	–	Bit[7:0]: Dark contrast enhancement Y Th3[15:8]
0x54C5	YTH1TARGET_3_L	–	–	Bit[7:0]: Dark contrast enhancement Y Th3[7:0]
0x54C6	SPRECTLIST_0_H	–	–	Bit[7:0]: B/R for D65[15:8]
0x54C7	SPRECTLIST_0_L	–	–	Bit[7:0]: B/R for D65[7:0]
0x54C8	SPRECTLIST_1_H	–	–	Bit[7:0]: B/R for CWF[15:8]
0x54C9	SPRECTLIST_1_L	–	–	Bit[7:0]: BB/R for CWF[7:0]
0x54CA	SPRECTLIST_2_H	–	–	Bit[7:0]: B/R for A[15:8]
0x54CB	SPRECTLIST_2_L	–	–	Bit[7:0]: B/R for A[7:0]
0x54CC	INVMLMS_D_0_0_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 00[15:8]
0x54CD	INVMLMS_D_0_0_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 00[7:0]
0x54CE	INVMLMS_D_0_1_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 01[15:8]
0x54CF	INVMLMS_D_0_1_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 01[7:0]
0x54D0	INVMLMS_D_0_2_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 02[15:8]
0x54D1	INVMLMS_D_0_2_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 02[7:0]

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address	register name	default value	R/W	description
0x54D2	INVMLMS_D_1_0_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 10[15:8]
0x54D3	INVMLMS_D_1_0_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 0[7:0]
0x54D4	INVMLMS_D_1_1_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 11[15:8]
0x54D5	INVMLMS_D_1_1_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 11[7:0]
0x54D6	INVMLMS_D_1_2_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 12[15:8]
0x54D7	INVMLMS_D_1_2_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 12[7:0]
0x54D8	INVMLMS_D_2_0_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 20[15:8]
0x54D9	INVMLMS_D_2_0_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 0[7:0]
0x54DA	INVMLMS_D_2_1_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 21[15:8]
0x54DB	INVMLMS_D_2_1_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 21[7:0]
0x54DC	INVMLMS_D_2_2_H	–	–	Bit[7:0]: SPD to LPD D65 matrix 22[15:8]
0x54DD	INVMLMS_D_2_2_L	–	–	Bit[7:0]: SPD to LPD D65 matrix 22[7:0]
0x54DE	INVMLMS_C_0_0_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 00[15:8]
0x54DF	INVMLMS_C_0_0_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 00[7:0]
0x54E0	INVMLMS_C_0_1_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 01[15:8]
0x54E1	INVMLMS_C_0_1_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 01[7:0]
0x54E2	INVMLMS_C_0_2_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 02[15:8]
0x54E3	INVMLMS_C_0_2_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 02[7:0]
0x54E4	INVMLMS_C_1_0_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 10[15:8]

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address	register name	default value	R/W	description
0x54E5	INVMLMS_C_1_0_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 0[7:0]
0x54E6	INVMLMS_C_1_1_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 11[15:8]
0x54E7	INVMLMS_C_1_1_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 11[7:0]
0x54E8	INVMLMS_C_1_2_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 12[15:8]
0x54E9	INVMLMS_C_1_2_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 12[7:0]
0x54EA	INVMLMS_C_2_0_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 20[15:8]
0x54EB	INVMLMS_C_2_0_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 0[7:0]
0x54EC	INVMLMS_C_2_1_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 21[15:8]
0x54ED	INVMLMS_C_2_1_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 21[7:0]
0x54EE	INVMLMS_C_2_2_H	–	–	Bit[7:0]: SPD to LPD CWF matrix 22[15:8]
0x54EF	INVMLMS_C_2_2_L	–	–	Bit[7:0]: SPD to LPD CWF matrix 22[7:0]
0x54F0	INVMLMS_A_0_0_H	–	–	Bit[7:0]: SPD to LPD A matrix 00[15:8]
0x54F1	INVMLMS_A_0_0_L	–	–	Bit[7:0]: SPD to LPD A matrix 00[7:0]
0x54F2	INVMLMS_A_0_1_H	–	–	Bit[7:0]: SPD to LPD A matrix 01[15:8]
0x54F3	INVMLMS_A_0_1_L	–	–	Bit[7:0]: SPD to LPD A matrix 01[7:0]
0x54F4	INVMLMS_A_0_2_H	–	–	Bit[7:0]: SPD to LPD A matrix 02[15:8]
0x54F5	INVMLMS_A_0_2_L	–	–	Bit[7:0]: SPD to LPD A matrix 02[7:0]
0x54F6	INVMLMS_A_1_0_H	–	–	Bit[7:0]: SPD to LPD A matrix 10[15:8]
0x54F7	INVMLMS_A_1_0_L	–	–	Bit[7:0]: SPD to LPD A matrix 0[7:0]
0x54F8	INVMLMS_A_1_1_H	–	–	Bit[7:0]: SPD to LPD A matrix 11[15:8]
0x54F9	INVMLMS_A_1_1_L	–	–	Bit[7:0]: SPD to LPD A matrix 11[7:0]
0x54FA	INVMLMS_A_1_2_H	–	–	Bit[7:0]: SPD to LPD A matrix 12[15:8]
0x54FB	INVMLMS_A_1_2_L	–	–	Bit[7:0]: SPD to LPD A matrix 12[7:0]

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address	register name	default value	R/W	description
0x54FC	INVMLMS_A_2_0_H	–	–	Bit[7:0]: SPD to LPD A matrix 20[15:8]
0x54FD	INVMLMS_A_2_0_L	–	–	Bit[7:0]: SPD to LPD A matrix 0[7:0]
0x54FE	INVMLMS_A_2_1_H	–	–	Bit[7:0]: SPD to LPD A matrix 21[15:8]
0x54FF	INVMLMS_A_2_1_L	–	–	Bit[7:0]: SPD to LPD A matrix 21[7:0]
0x5500	INVMLMS_A_2_2_H	–	–	Bit[7:0]: SPD to LPD A matrix 22[15:8]
0x5501	INVMLMS_A_2_2_L	–	–	Bit[7:0]: SPD to LPD A matrix 22[7:0]
0x5502	TARGETNUM	–	–	Target Number 00: AA mode 01: AB mode 10: ABC mode
0x5503	IDLEWORKMODE	–	–	Idle Work Mode
0x5504	VTS_H	–	–	Bit[7:0]: VTS[15:8]
0x5505	VTS_L	–	–	Bit[7:0]: VTS[7:0]
0x5506	LOGTARGETLD_H	–	–	Bit[7:0]: Low dynamic range scene target[15:8]
0x5507	LOGTARGETLD_L	–	–	Bit[7:0]: Low dynamic range scene target[7:0]
0x5508	DYNAMICTARGETENABLE	–	–	Dynamic Change Target Function Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5509	LDTH0	–	–	Dynamic Change Low Threshold
0x550A	LDTH1	–	–	Dynamic Change High Threshold
0x550B~ 0x5539	RSVD	–	–	Reserved

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4.8 linear stretch

Stretch is designed to automatically enhance the contrast of images. As shown in **figure 4-22**, the input signal between low level and high level will be stretched to [0, 1023]. Input signal below low level will be cut to 0 and input signal over high level will be saturated to 1023. The stretch module is enabled by default and can be disabled by register 0x5001[2].

In auto mode (0x5B00[0]), high and low level will be adjusted according to image content. In manual mode (0x5B00[1]), the high level and low level can be manually set by registers 0x5B08~0x5B0A. The pixel numbers below the low level and above the high level will be cut to 0 or 1023 respectively, the details in these regions will be lost.

There are two thresholds (stretch_thres1 and stretch_thres2) which are used to control the pixels below current low level and above the current high level calculated for every frame in auto mode.

If the pixel numbers below the low level is larger than (stretch_thres1+ stretch_minimum/2), the current low level will reduce by register 0x5B04[3:0] until it reach min low level defined in register 0x5B01.

If the pixels' signal below the low level is lower than (stretch_thres1-stretch_minimum/2), the current low level will increase by register 0x5B04[3:0] until it reach the max low level defined in register 0x5B02.

This ensures that pixels cut to 0 can be controlled in stable state.

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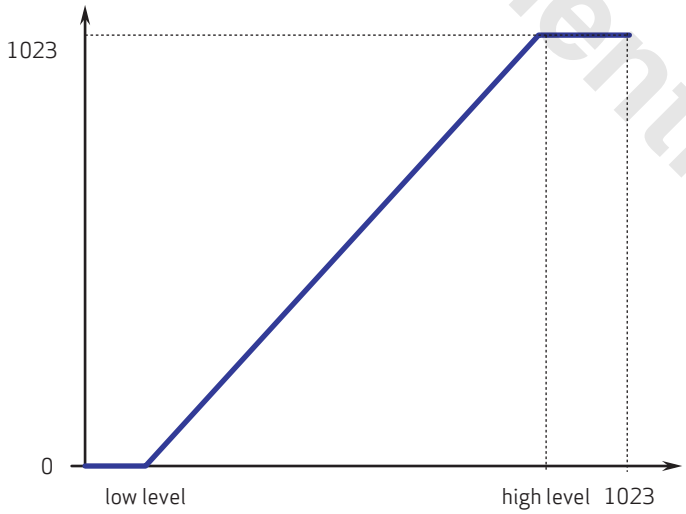
figure 4-22 stretch graph



$$y = \begin{cases} 0 \quad if\ x \le LowLevel \\ \dfrac{1023 \times (x - LowLevel)}{(HighLevel - LowLevel)} \quad if\ LowLevel < x < HighLevel \\ 1023\ if\ x \ge hHighLevel \end{cases}$$

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table 4-18 stretch control registers

address	register name	default value	R/W	description
0x5B00	STRETCH_CTRL0_O	0x09	RW	Bit[3:2]: Stretch minimum register Real stretch minimum value is: 00: 1024 01: 2048 10: 4096 11: 8192 Bit[1]: Stretch manual 0: Disable 1: Enable Bit[0]: Stretch auto 0: Disable 1: Enable
0x5B01	STRETCH_CTRL1_0_O	0x00	RW	Bit[4:0]: Stretch minimum low level
0x5B02	STRETCH_CTRL1_1_O	0x10	RW	Bit[4:0]: Stretch maximum low level
0x5B03	STRETCH_CTRL2_O	0x10	RW	Bit[4:0]: Stretch minimum high level
0x5B04	STRETCH_CTRL3_O	0x41	RW	Bit[7:4]: Stretch step2 value Bit[3:0]: Stretch step1 value
0x5B05	STRETCH_CTRL4_O	0x10	RW	Bit[7:0]: Stretch low level initial value[7:0]
0x5B06	STRETCH_CTRL5_O	0x03	RW	Bit[1:0]: Stretch high level initial value[9:8]
0x5B07	STRETCH_CTRL6_O	0xFF	RW	Bit[7:0]: Stretch high level initial value[7:0]
0x5B08	STRETCH_CTRL7_O	0x10	RW	Bit[7:0]: Current low level manual value[7:0]
0x5B09	STRETCH_CTRL8_O	0x03	RW	Bit[1:0]: Current high level manual value[9:8]
0x5B0A	STRETCH_CTRL9_O	0xFF	RW	Bit[7:0]: Current high level manual value[7:0]
0x5B0B	STRETCH_CTRLA_O	0x00	RW	Bit[1:0]: Stretch threshold[17:16]
0x5B0C	STRETCH_CTRLB_O	0x3B	RW	Bit[7:0]: Stretch threshold 1[15:8]
0x5B0D	STRETCH_CTRLC_O	0xC4	RW	Bit[7:0]: Stretch threshold 1[7:0]
0x5B0E	STRETCH_CTRLD_O	0x00	RW	Bit[1:0]: Stretch threshold 2[17:16]
0x5B0F	STRETCH_CTRLE_O	0x3B	RW	Bit[7:0]: Stretch threshold 2[15:8]
0x5B10	STRETCH_CTRLF_O	0xC4	RW	Bit[7:0]: Stretch threshold 2[7:0]
0x5B11	CUR_LOWLVL_I	–	R	Bit[7:0]: Current low level[7:0]
0x5B12	CUR_HIGHLVL_H_I	–	R	Bit[1:0]: Current high level[9:8]
0x5B13	CUR_HIGHLVL_L_I	–	R	Bit[7:0]: Current high level[7:0]
0x5B14	STRETCH_GAIN_H_I	–	R	Bit[0]: Stretch gain value[8]
0x5B15	STRETCH_GAIN_L_I	–	R	Bit[7:0]: Stretch gain value[7:0]

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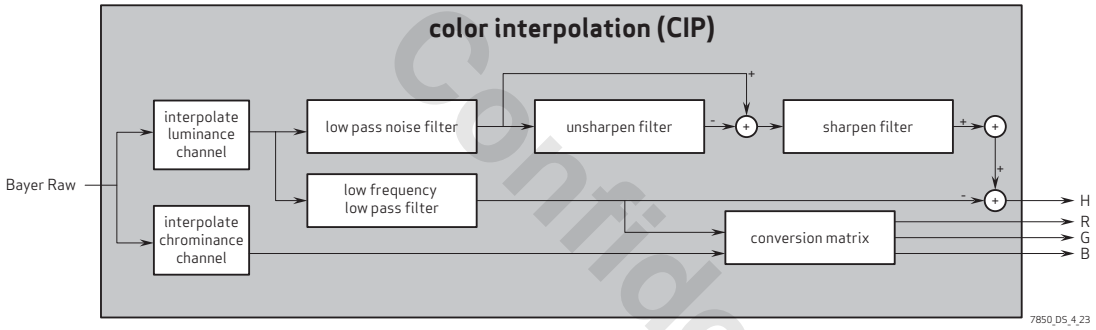
4.9 color interpolation (CIP)

The next step in processing is to convert the Bayer format to an RGB per pixel format. The two missing color values in each pixel are interpolated from the neighboring pixels. CIP also implements other functions such as de-noise, edge sharpening and binning/sub-sampling artifacts correction. The noise filtering and sharpness enhancement is performed in the luminance channel only (see **figure 4-23**). The CIP is enabled by default and can be disabled through register 0x5001[7:6]. The input of the CIP block is the Bayer RAW data and the output of the block is R, G and B signal of each pixel, plus a high frequency luminance signal H.

figure 4-23 CIP block diagram



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4.9.1 color interpolation

There are two parameters that will change the color aliasing in high frequency region and green channel interpolation on color edges.

- Anti_aliasing: (register 0x5C90[6]): when set to 1, it will help reduce color aliasing in regions with horizontal or vertical high frequency details.
- Cip_option: (register 0x5C90[4]): when set to 1, it will help reduce black dot artifacts in diagonal color edges, but it may also introduce color aliasing in regions with high frequency in diagonal directions.

4.9.2 DNS in CIP

Similar to other DNS modules, there is a noise list to control the de-noise level at different AGC gain. Because it is applied on the linear domain, it also has a slope parameter to increase the de-noise level in light tone. Some sensors have differences between Gb and Gr channels that will cause horizontal, vertical, or grid fixed pattern noise in final images. Two parameters are introduced to reduce the difference between Gb and Gr channels.

- Noise_y_slp: (register 0x5C80[7:4]) in linear domain, the shot noise will increase with the signal level, so in same linear raw image, the dark tone has lower noise level than the mid tone and light tone. This parameter is used to increase the DNS level with the signal level. With a larger value, it will reduce more noise in light tone.
- Gbgr_rem_enable: (register 0x5C81[0]) set it to 1 will enable the removal of Gb/Gr difference.
- Gbgr_shift: (register 0x5C81[4:1]) when set to n, the gb/gr difference will be divided by 2n.

4.9.3 edge sharpening

CIP still includes two edge sharpening methods. The first method is the commonly used in un-sharp mask, which is applied equally everywhere in the image. The second method will locally adjust the edge sharpness, which is named as local-sharpen.

The basic idea of the un-sharp mask method is to amplify the high frequency component of image signal and then add it back to enhance the edge. It is controlled by two parameters: one is the sharpening level, which is the gain used to amplify the high frequency. The other is a threshold, which is used to control the small high frequency that will not be amplified. When the sensor gain increased, the noise level will also increase. So the sharpening level and the threshold should adjust with gain to get better image quality. As shown in **figure 4-24**, when the sensor gain is lower than min_sharpen_gain, the sharpening level will be max_sharpen and the threshold will be min_detail. When sensor gain is larger than max_sharpen_gain, the sharpening level will be min_sharpen and the threshold will be max_detail. When the sensor gain is within the range of [min_sharpen_gain, max_sharpen_gain], the sharpening level and the threshold will be linear interpolated.

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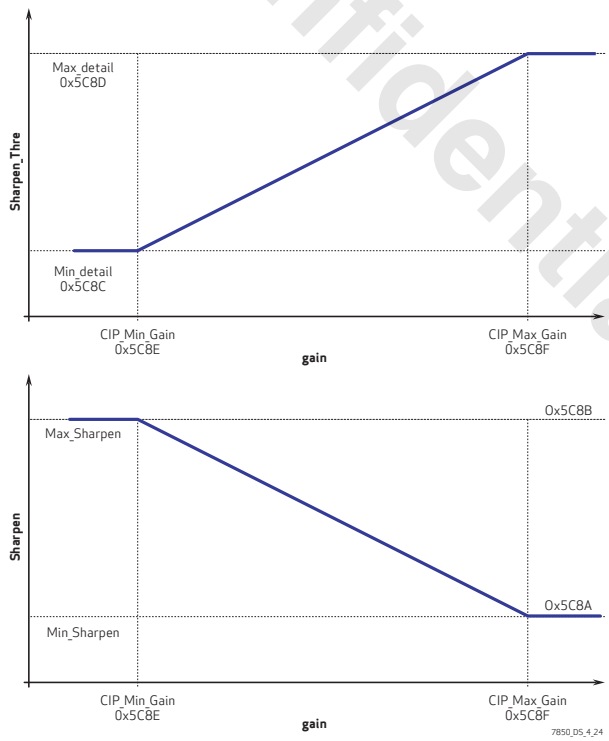
figure 4-24 sharpen curve



Unlike the un-sharp mask method, the local sharpening will increase the sharpness without generating the overshoot artifacts.

- local_sharpen: (register 0x5C80[3:0]) using larger local_sharpen, it will get more sharp edges, but too large parameter may also generate zigzag artifacts.

table 4-19 CIP control registers

address	register name	default value	R/W	description
0x5C80	R_CIP_CTRL_0	0x80	RW	Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x5C81	R_CIP_CTRL_1	0x00	RW	Bit[4:1]: GbGr shift Bit[0]: GbGr remove enable
0x5C82	R_CIP_NOISE_LIST_0	0x00	RW	Bit[7:0]: Noise List[0]
0x5C83	R_CIP_NOISE_LIST_1	0x00	RW	Bit[7:0]: Noise List[1]
0x5C84	R_CIP_NOISE_LIST_2	0x00	RW	Bit[7:0]: Noise List[2]
0x5C85	R_CIP_NOISE_LIST_3	0x00	RW	Bit[7:0]: Noise List[3]
0x5C86	R_CIP_NOISE_LIST_4	0x00	RW	Bit[7:0]: Noise List[4]
0x5C87	R_CIP_NOISE_LIST_5	0x00	RW	Bit[7:0]: Noise List[5]
0x5C88	R_CIP_NOISE_LIST_6	0x00	RW	Bit[7:0]: Noise List[6]
0x5C89	R_CIP_NOISE_LIST_7	0x00	RW	Bit[7:0]: Noise List[7]
0x5C8A	R_CIP_MIN_SHARPEN	0x00	RW	Bit[5:0]: Minimum sharpen
0x5C8B	R_CIP_MAX_SHARPEN	0x0C	RW	Bit[5:0]: Maximum sharpen
0x5C8C	R_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Minimum detail
0x5C8D	R_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Maximum detail
0x5C8E	R_CIP_MIN_SHARPEN_GAIN	0x02	RW	Bit[7:0]: Minimum sharpen gain
0x5C8F	R_CIP_MAX_SHARPEN_GAIN	0x10	RW	Bit[7:0]: Maximum sharpen gain
0x5C90	R_CIP_CTRL_2	0x60	RW	Bit[6]: Anti aliasing Bit[5]: FixH binning enable Bit[4]: CIP option Bit[3:2]: Binning pattern Bit[1:0]: Binning mode
0x5C91	R_CIP_EOF_DELAY	0x28	RW	Bit[6:0]: Number of EOF signal delay cycles
0x5C92	R_CIP_AF_FILTER_COEF_0	0x00	RW	Bit[7:0]: AF filter coefficient[0]
0x5C93	R_CIP_AF_FILTER_COEF_1	0x00	RW	Bit[7:0]: AF filter coefficient[1]
0x5C94	R_CIP_AF_FILTER_COEF_2	0x00	RW	Bit[7:0]: AF filter coefficient[2]
0x5C95	R_CIP_AF_FILTER_COEF_3	0x00	RW	Bit[7:0]: AF filter coefficient[3]
0x5C96	R_CIP_CTRL_3	0x10	RW	Bit[7]: Anti flickering enable Bit[6:5]: Reserved Bit[4:0]: Sharpen V coefficient

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4.10 color matrix (CMX)

Due to spectrum crosstalk, a color correction matrix (CCM) must be applied on the R, G and B values of each pixel to improve the color fidelity. The optimal color correction matrix depends on pixel QE spectrum response and the spectrum of the light source. To optimize for sensor crosstalk, the OV7850 can use three color matrices calibrated with three different color temperatures. Alternatively, a single matrix can be used for all color temperatures (0x5D31[1]). The CMX module is enabled by register 0x5002[0].

The following equation shows the corrected RGB vector on left-hand side, the right-hand side is 3x3 matrix multiplied by the white balanced sensor RGB vector. The matrix should be balanced; otherwise, the white point in sensor RGB space cannot be transformed into the white point in target RGB space. So, one 3x3 matrix only needs six independent parameters (c00, c01, …, c21). The parameters can be read from registers 0x5D36~0x5D41.

$$\begin{bmatrix} B' \\ G' \\ R' \end{bmatrix} = \frac{1}{1024} \begin{bmatrix} 1024 + C_{00} + C_{01} & -C_{00} & -C_{01} \\ -C_{10} & 1024 + C_{10} + C_{11} & -C_{11} \\ -C_{20} & -C_{21} & 1024 + C_{20} + C_{21} \end{bmatrix} \begin{bmatrix} B \\ G \\ R \end{bmatrix}$$

The current color matrix is automatically estimated based on current CT calculated from the AWB gain. CT is defined as:

CT = (blue channel AWB gain X 128)/(red channel AWB gain)

In day light, the CT value will be smaller than the CT value in incandescent light. Three thresholds can be defined (ctlist0, ctlist1, ctlist2 in the following equation), which will divide the CT space into four regions. The current matrix can be calculated based on which region current CT belong to.

$$M_{3x3} = \begin{cases} D_{3x3}, ct \le ct_0 \\ D_{3x3} + \dfrac{(C_{3x3} - D_{3x3})(ct - ct_0)}{ct_1 - ct_0}, ct_0 < ct \le ct_1 \\ C_{3x3} + \dfrac{(A_{3x3} - C_{3x3})(ct - ct_0)}{ct_1 - ct_0}, ct_1 < ct \le ct_2 \\ A_{3x3}, ct_2 < ct \end{cases}$$

note 1 C: CCM usually calibrated in cool white flourecent light (CWF) , 0x5D18 -0x5D23
D: CCM usually calibrate in Day light 0x5D00-5D0B
A: CCM usually calibrate in A light 0x5D0C-0x5D17
M: CCM used at current CT, 0x0x5D36-0x5D41
ct0: CT threshold for D 0x5D28-0x5D29
ct1: CT threshold for C 0x5D2A-0x5D2B
ct2: CT threshold for A 0x5D2C -0x5D2D

The values in the CCMs are absolute values. The sign for the six parameters given for each CCM is given in registers 0x5D2E, 0x5D2F and 0x5D30 for D, A, and CWF light.

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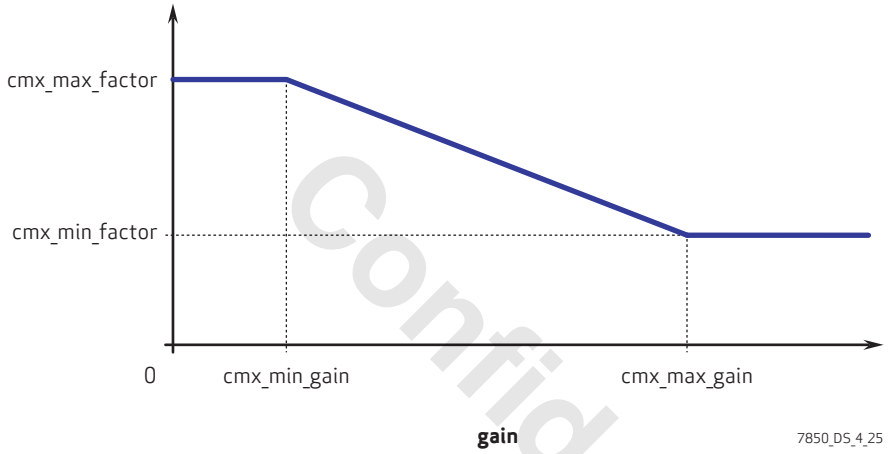
When the sensor gain is high, the OV7850 can automatically reduce saturation enabled by register 0x5D31[0]. When the sensor gain is between cmx_min_gain (0x5D34) and cmx_max_gain (0x5D35), the factor will be linearly interpolated as shown in **figure 4-25**. A factor of 64 means the color saturation will be the same as the original color. A factor smaller than 64 will reduce the color saturation. A factor of 0 will reduce color image to a black/white image.

figure 4-25 CMX curve diagram



Manual control of the BR gain is enabled though 0x5D24[4]. The B and R gain is 12-bit wide and given by registers {0x5D25[3:0],0x5D25} for B gain and registers {0x5D26[3:0],0x5D25} for R gain.

table 4-20 CMX control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5D00	R_CMX_CTRL0_O	0x03	RW	Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D01	R_CMX_CTRL1_O	0xF2	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in day color temperature mode
0x5D02	R_CMX_CTRL2_O	0x00	RW	Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in day color temperature mode
0x5D03	R_CMX_CTRL3_O	0x39	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in day color temperature mode
0x5D04	R_CMX_CTRL4_O	0x01	RW	Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B channel in day color temperature mode

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table 4-20 CMX control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5D05	R_CMX_CTRL5_O	0xAF	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in day color temperature mode
0x5D06	R_CMX_CTRL6_O	0x01	RW	Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in day color temperature mode
0x5D07	R_CMX_CTRL7_O	0x42	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in day color temperature mode
0x5D08	R_CMX_CTRL8_O	0x00	RW	Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in day color temperature mode
0x5D09	R_CMX_CTRL9_O	0x99	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in day color temperature mode
0x5D0A	R_CMX_CTRLA_O	0x01	RW	Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in day color temperature mode
0x5D0B	R_CMX_CTRLB_O	0xCE	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in day color temperature mode
0x5D0C	R_CMX_CTRLC_O	0x06	RW	Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D0D	R_CMX_CTRLD_O	0x80	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in A color temperature mode
0x5D0E	R_CMX_CTRLE_O	0x00	RW	Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in A color temperature mode
0x5D0F	R_CMX_CTRLF_O	0x5B	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in A color temperature mode
0x5D10	R_CMX_CTRL10_O	0x01	RW	Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B channel in A color temperature mode
0x5D11	R_CMX_CTRL11_O	0x00	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in A color temperature mode

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table 4-20 CMX control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5D12	R_CMX_CTRL12_O	0x01	RW	Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in A color temperature mode
0x5D13	R_CMX_CTRL13_O	0xDD	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in A color temperature mode
0x5D14	R_CMX_CTRL14_O	0x00	RW	Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in A color temperature mode
0x5D15	R_CMX_CTRL15_O	0x7F	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in A color temperature mode
0x5D16	R_CMX_CTRL16_O	0x03	RW	Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D17	R_CMX_CTRL17_O	0x22	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in A color temperature mode
0x5D18	R_CMX_CTRL18_O	0x05	RW	Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in CWF color temperature mode
0x5D19	R_CMX_CTRL19_O	0x46	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in CWF color temperature mode
0x5D1A	R_CMX_CTRL1A_O	0x00	RW	Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in CWF color temperature mode
0x5D1B	R_CMX_CTRL1B_O	0x53	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in CWF color temperature mode
0x5D1C	R_CMX_CTRL1C_O	0x01	RW	Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B Channel in CWF color temperature mode
0x5D1D	R_CMX_CTRL1D_O	0x08	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in CWF color temperature mode
0x5D1E	R_CMX_CTRL1E_O	0x01	RW	Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in CWF color temperature mode

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table 4-20 CMX control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x5D1F	R_CMX_CTRL1F_O	0x43	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in CWF color temperature mode
0x5D20	R_CMX_CTRL20_O	0x00	RW	Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in CWF color temperature mode
0x5D21	R_CMX_CTRL21_O	0x81	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in CWF color temperature mode
0x5D22	R_CMX_CTRL22_O	0x01	RW	Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in CWF color temperature mode
0x5D23	R_CMX_CTRL23_O	0x55	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in CWF color temperature mode
0x5D24	R_CMX_CTRL24_O	0x01	RW	Bit[4]: CMX BR gain manual Bit[3:0]: AWB B gain[11:8] 0: Disable 1: Enable
0x5D25	R_CMX_CTRL25_O	0x00	RW	Bit[7:0]: AWB B gain[7:0]
0x5D26	R_CMX_CTRL26_O	0x01	RW	Bit[3:0]: AWB R gain[11:8]
0x5D27	R_CMX_CTRL27_O	0x00	RW	Bit[7:0]: AWB R gain[7:0]
0x5D28	R_CMX_CTRL28_O	0x00	RW	CMX Color Temperature Threshold Bit[1:0]: List_0[9:8] for day color temperature mode
0x5D29	R_CMX_CTRL29_O	0x72	RW	CMX Color Temperature Threshold Bit[7:0]: List_0[7:0] for day color temperature mode
0x5D2A	R_CMX_CTRL2A_O	0x00	RW	CMX Color Temperature Threshold Bit[1:0]: List_1[9:8] for CWF color temperature mode
0x5D2B	R_CMX_CTRL2B_O	0xBA	RW	CMX Color Temperature Threshold Bit[7:0]: List_1[7:0] for CWF color temperature mode
0x5D2C	R_CMX_CTRL2C_O	0x01	RW	CMX Color Temperature Threshold Bit[1:0]: List_2[9:8] for A color temperature mode
0x5D2D	R_CMX_CTRL2D_O	0x37	RW	CMX Color Temperature Threshold Bit[7:0]: List_2[7:0] for A color temperature mode
0x5D2E	R_CMX_CTRL2E_O	0x02	RW	Six Coefficient Signs in Day Color Temperature Mode, 0 Indicates Negative

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table 4-20 CMX control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5D2F	R_CMX_CTRL2F_O	0x00	RW	Six Coefficient Signs in A Color Temperature Mode, 0 Indicates Negative
0x5D30	R_CMX_CTRL30_O	0x00	RW	Six Coefficient Signs in CWF Color Temperature Mode, 0 Indicates Negative
0x5D31	R_CMX_CTRL31_O	0x01	RW	Bit[1]: CT based color matrix 0: Always use single matrix D in all color temperatures 1: Enable CT based color matrix Bit[0]: CMX auto factor enable signal 0: Do not reduce color saturation when large sensor gain 1: Automatically reduce color saturation when large sensor gain, see 0x5D32 and 0x5D33
0x5D32	R_CMX_CTRL32_O	0x64	RW	CMX Maximum Factor Value Factor used when sensor gain is below CMX minimum gain value in register 0x5D34
0x5D33	R_CMX_CTRL33_O	0x64	RW	CMX Minimum Factor Value Factor used when sensor gain is exceeding CMX maximum gain value in register 0x5D35
0x5D34	R_CMX_CTRL34_O	0x07	RW	CMX Minimum Gain Value
0x5D35	R_CMX_CTRL35_O	0x15	RW	CMX Maximum Gain Value
0x5D36	ABS_CMX00_H_I	–	R	Bit[3:0]: CMX00[11:8] Read register of color matrix for G channel
0x5D37	ABS_CMX00_L_I	–	R	Bit[7:0]: CMX00[7:0] Read register of color matrix for G channel
0x5D38	ABS_CMX01_H_I	–	R	Bit[3:0]: CMX01[11:8] Read register of color matrix for R channel
0x5D39	ABS_CMX01_L_I	–	R	Bit[7:0]: CMX01[7:0] Read register of color matrix for R channel
0x5D3A	ABS_CMX10_H_I	–	R	Bit[3:0]: CMX10[11:8] Read register of color matrix for B channel
0x5D3B	ABS_CMX10_L_I	–	R	Bit[7:0]: CMX10[7:0] Read register of color matrix for B channel

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table 4-20 CMX control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x5D3C	ABS_CMX11_H_I	–	R	Bit[3:0]: CMX11[11:8] Read register of color matrix for R channel
0x5D3D	ABS_CMX11_L_I	–	R	Bit[7:0]: CMX11[7:0] Read register of color matrix for R channel
0x5D3E	ABS_CMX20_H_I	–	R	Bit[3:0]: CMX20[11:8] Read register of color matrix for B channel
0x5D3F	ABS_CMX20_L_I	–	R	Bit[7:0]: CMX20[7:0] Read register color matrix for B channel
0x5D40	ABS_CMX21_H_I	–	R	Bit[3:0]: CMX21[11:8] Read register of color matrix for G channel
0x5D41	ABS_CMX21_L_I	–	R	Bit[7:0]: CMX21[7:0] Read register of color matrix for G channel
0x5D42	SIGN_CMX	–	R	Read Register for Matrix Six Value Signs, 0 Indicates Negative

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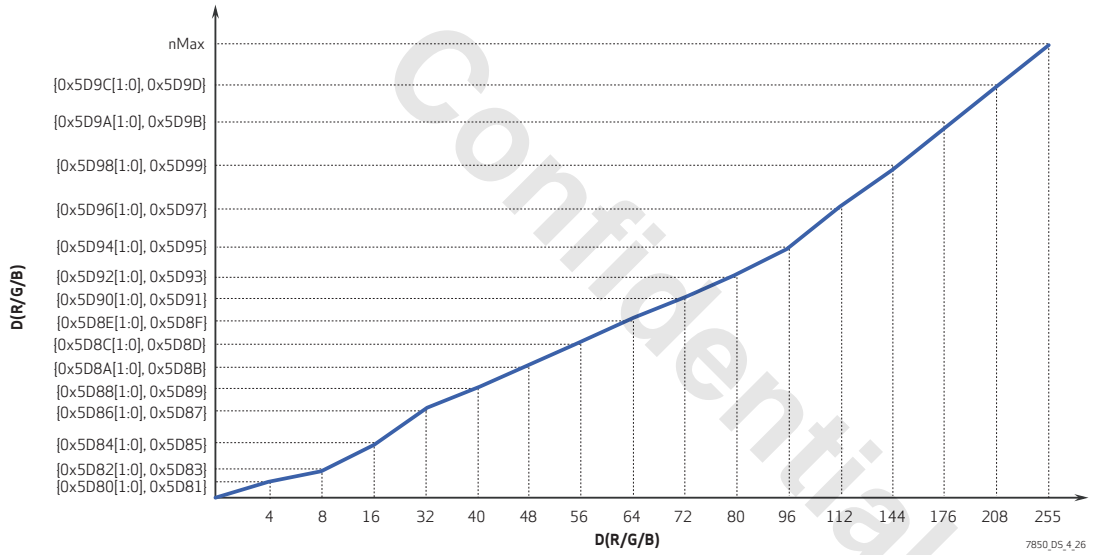
4.11 RGB gamma

Gamma correction is used to compensate for the nonlinearity in intensity reproduction of the display device. The gamma correction must increase with the dynamic range to maintain the same shadow of gray, similar to the display. The gamma correction is enabled by default and can be disabled by register 0x5002[1].

A gamma curve is used for R/G/B channel correction. **figure 4-26** shows the gamma curve used for different D. Registers 0x5D80~0x5D9D define the gamma curve list.

figure 4-26 gamma curve diagram



D'=Y[i-1]+((D-X[i-1])*(Y[i]-Y[i-1]))/(X[i]-X[i-1])

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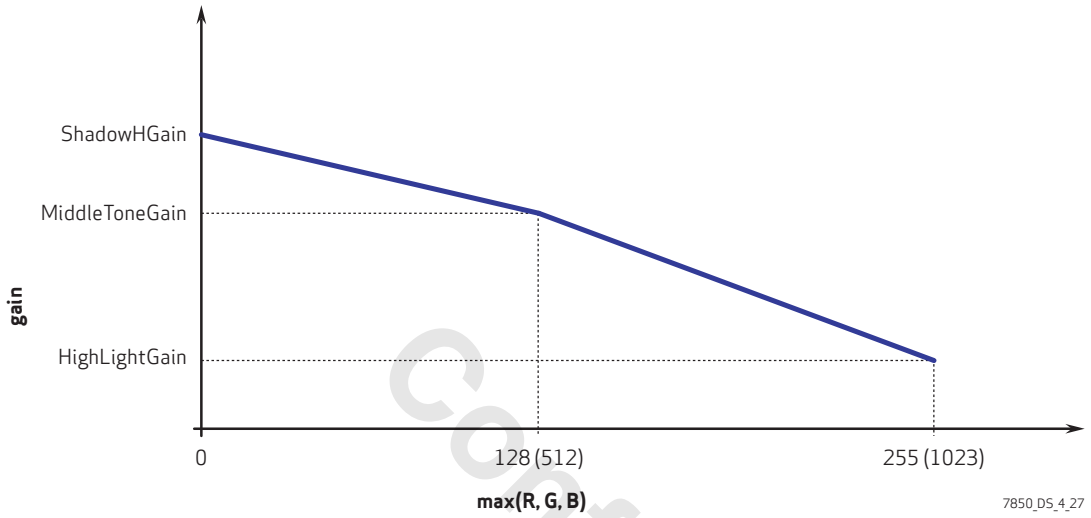
figure 4-27 gamma curve diagram



A gain will be applied to Y channel based on the maximum R, G or B channel data. Shadow H gain is calculated based on the real gain and register 0x5DBC defines the maximum value of shadow H gain. Register 0x5DBD defines middle tone H gain and register 0x5DBE defines high light H gain. It provides the user a method to adjust the noise level in shadow, mid-tone, and high light.

table 4-21 RGB gamma control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5D80	R_Y_LIST_00_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[0][9:8]
0x5D81	R_Y_LIST_00_AUTO_L	0x0E	RW	Bit[7:0]: Gamma curve Y list[0][7:0]
0x5D82	R_Y_LIST_01_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[1][9:8]
0x5D83	R_Y_LIST_01_AUTO_L	0x1A	RW	Bit[7:0]: Gamma curve Y list[1][7:0]
0x5D84	R_Y_LIST_02_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[2][9:8]
0x5D85	R_Y_LIST_02_AUTO_L	0x31	RW	Bit[7:0]: Gamma curve Y list[2][7:0]
0x5D86	R_Y_LIST_03_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[3][9:8]
0x5D87	R_Y_LIST_03_AUTO_L	0x5A	RW	Bit[7:0]: Gamma curve Y list[3][7:0]
0x5D88	R_Y_LIST_04_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[4][9:8]
0x5D89	R_Y_LIST_04_AUTO_L	0x69	RW	Bit[7:0]: Gamma curve Y list[4][7:0]
0x5D8A	R_Y_LIST_05_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[5][9:8]
0x5D8B	R_Y_LIST_05_AUTO_L	0xD7	RW	Bit[7:0]: Gamma curve Y list[5][7:0]

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table 4-21 RGB gamma control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5D8C	R_Y_LIST_06_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[6][9:8]
0x5D8D	R_Y_LIST_06_AUTO_L	0xE8	RW	Bit[7:0]: Gamma curve Y list[6][7:0]
0x5D8E	R_Y_LIST_07_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[7][9:8]
0x5D8F	R_Y_LIST_07_AUTO_L	0x88	RW	Bit[7:0]: Gamma curve Y list[7][7:0]
0x5D90	R_Y_LIST_08_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[8][9:8]
0x5D91	R_Y_LIST_08_AUTO_L	0x8F	RW	Bit[7:0]: Gamma curve Y list[8][7:0]
0x5D92	R_Y_LIST_09_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[9][9:8]
0x5D93	R_Y_LIST_09_AUTO_L	0x96	RW	Bit[7:0]: Gamma curve Y list[9][7:0]
0x5D94	R_Y_LIST_10_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[10][9:8]
0x5D95	R_Y_LIST_10_AUTO_L	0xA3	RW	Bit[7:0]: Gamma curve Y list[10][7:0]
0x5D96	R_Y_LIST_11_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[11][9:8]
0x5D97	R_Y_LIST_11_AUTO_L	0xAF	RW	Bit[7:0]: Gamma curve Y list[11][7:0]
0x5D98	R_Y_LIST_12_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[12][9:8]
0x5D99	R_Y_LIST_12_AUTO_L	0xC4	RW	Bit[7:0]: Gamma curve Y list[12][7:0]
0x5D9A	R_Y_LIST_13_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[13][9:8]
0x5D9B	R_Y_LIST_13_AUTO_L	0xB0	RW	Bit[7:0]: Gamma curve Y list[13][7:0]
0x5D9C	R_Y_LIST_14_AUTO_H	0x00	RW	Bit[1:0]: Gamma curve Y list[14][9:8]
0x5D9D	R_Y_LIST_14_AUTO_L	0xD0	RW	Bit[7:0]: Gamma curve Y list[14][7:0]
0x5D9E	R_Y_LIST_00_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[0][9:8]
0x5D9F	R_Y_LIST_00_MANUAL_L	0x04	RW	Bit[7:0]: Manual gamma curve Y list[0][7:0]
0x5DA0	R_Y_LIST_01_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[1][9:8]
0x5DA1	R_Y_LIST_01_MANUAL_L	0x08	RW	Bit[7:0]: Manual gamma curve Y list[1][7:0]
0x5DA2	R_Y_LIST_02_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[2][9:8]
0x5DA3	R_Y_LIST_02_MANUAL_L	0x10	RW	Bit[7:0]: Manual gamma curve Y list[2][7:0]
0x5DA4	R_Y_LIST_03_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[3][9:8]
0x5DA5	R_Y_LIST_03_MANUAL_L	0x20	RW	Bit[7:0]: Manual gamma curve Y list[3][7:0]
0x5DA6	R_Y_LIST_04_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[4][9:8]
0x5DA7	R_Y_LIST_04_MANUAL_L	0x28	RW	Bit[7:0]: Manual gamma curve Y list[4][7:0]
0x5DA8	R_Y_LIST_05_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[5][9:8]
0x5DA9	R_Y_LIST_05_MANUAL_L	0x30	RW	Bit[7:0]: Manual gamma curve Y list[5][7:0]

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table 4-21 RGB gamma control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5DAA	R_Y_LIST_06_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[6][9:8]
0x5DAB	R_Y_LIST_06_MANUAL_L	0x38	RW	Bit[7:0]: Manual gamma curve Y list[6][7:0]
0x5DAC	R_Y_LIST_07_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[7][9:8]
0x5DAD	R_Y_LIST_07_MANUAL_L	0x40	RW	Bit[7:0]: Manual gamma curve Y list[7][7:0]
0x5DAE	R_Y_LIST_08_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[8][9:8]
0x5DAF	R_Y_LIST_08_MANUAL_L	0x48	RW	Bit[7:0]: Manual gamma curve Y list[8][7:0]
0x5DB0	R_Y_LIST_09_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[9][9:8]
0x5DB1	R_Y_LIST_09_MANUAL_L	0x50	RW	Bit[7:0]: Manual gamma curve Y list[9][7:0]
0x5DB2	R_Y_LIST_10_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[10][9:8]
0x5DB3	R_Y_LIST_10_MANUAL_L	0x60	RW	Bit[7:0]: Manual gamma curve Y list[10][7:0]
0x5DB4	R_Y_LIST_11_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[11][9:8]
0x5DB5	R_Y_LIST_11_MANUAL_L	0x70	RW	Bit[7:0]: Manual gamma curve Y list[11][7:0]
0x5DB6	R_Y_LIST_12_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[12][9:8]
0x5DB7	R_Y_LIST_12_MANUAL_L	0x90	RW	Bit[7:0]: Manual gamma curve Y list[12][7:0]
0x5DB8	R_Y_LIST_13_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[13][9:8]
0x5DB9	R_Y_LIST_13_MANUAL_L	0xB0	RW	Bit[7:0]: Manual gamma curve Y list[13][7:0]
0x5DBA	R_Y_LIST_14_MANUAL_H	0x00	RW	Bit[1:0]: Manual gamma curve Y list[14][9:8]
0x5DBB	R_Y_LIST_14_MANUAL_L	0xD0	RW	Bit[7:0]: Manual gamma curve Y list[14][7:0]
0x5DBC	R_MAX_SHADOW_H_GAIN	0xFF	RW	Bit[7:0]: Gamma maximum shadow h gain
0x5DBD	R_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Middle tone h gain
0x5DBE	R_HIGH_LIGHT_H_GAIN	0x10	RW	Bit[7:0]: High light h gain
0x5DBF	R_PARA_MANUAL_EN	0x00	RW	Manual Gamma Parameter Enable

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4.12 RGB2YUV

One of the last modules in the ISP pipeline is to convert data from RGB to YUV data path, enabled by default and can be disabled by 0x5002[3]. The RGB data is noise filtered before conversion and the YUV data is filtered after conversion.

$$\begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix} = M \times \begin{bmatrix} B \\ G \\ R \end{bmatrix} + \begin{bmatrix} 0 \\ H \\ H \end{bmatrix}$$

$$M = \begin{bmatrix} 29 & 150 & 77 \\ 128 & -85 & -43 \\ -21 & -107 & 128 \end{bmatrix} / 256$$

note H=128 for 8-bit YUV or 512 for 10-bit YUV

4.13 output format

Except for the fully processed YUV format, the image processor can also bypass some processing to output RAW data. The output format is selected by registers 0x4300 and 0x3024.

table 4-22 output control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	CTRL00	0x30	RW	Bit[7:4]: data_type 0000: raw_en 0001: y8_en 0011: yuv422_en 1111: byp_fmt Bit[3:0]: Pixel order control 00: YUYV 01: YVYU 10: UYVY 11: VYUY

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table 4-22 output control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4301	CTRL01	0x04	RW	Bit[7:6]: Reserved Bit[5]: Output format option2 for raw_x3 and RAW8 or 8-bit YUV422 Bit[4:3]: raw_type 00: raw_x1 01: raw_x2 1x: raw_x3 Bit[2:0]: raw_sel If raw_type == raw_x1: 000: {data1} 001: {data2} 010: {data3} If raw_type == raw_x2: 000: {data1,data2} 001: {data2,data3} 010: {data1,data3} 100: {data2,data1} 101: {data3,data2} 110: {data3,data1} If raw_type == raw_x3: 000: {data1,data2,data3} 001: {data1,data3,data2} 010: {data2,data1,data3} 011: {data2,data3,data1} 100: {data3,data1,data2} 101: {data3,data2,data1}
0x4302~ 0x4309	RSVD	–	–	Reserved

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4.14 window

The input window for ISP can be configured. This option is disabled by default but can be enabled by register bit 0x5003[6]. The required top, left, width and height information is put in registers {0x5012[1:0], 0x5013}, {0x5014[1:0], 0x5015}, {0x5016[1:0], 0x5017} and {0x5018[1:0], 0x5019}.

The ISP output window can be enable/disabled by 0x5003[7]. It is enabled by default. The output window x-offset, y-offset, width and height values are controlled by sensor core by default, but can be manually set by:

x-offset {0x5F00[1:0], 0x5F01}

y-offset {0x5F02[1:0], 0x5F03}

width {0x5F04[1:0], 0x5F05}

height {0x5F06[1:0], 0x5F07}

The manual options are enabled through register 0x5F08[0].

table 4-23 ISP window registers

address	register name	default value	R/W	description
0x5F00	R_CTRL00	0x00	RW	Bit[7:0]: Manual X start coordinate[15:8]
0x5F01	R_CTRL01	0x00	RW	Bit[7:0]: Manual X start coordinate[7:0]
0x5F02	R_CTRL02	0x00	RW	Bit[7:0]: Manual Y start coordinate[15:8]
0x5F03	R_CTRL03	0x00	RW	Bit[7:0]: Manual Y start coordinate[7:0]
0x5F04	R_CTRL04	0x02	RW	Bit[7:0]: Manual window width[15:8]
0x5F05	R_CTRL05	0xF0	RW	Bit[7:0]: Manual window width[7:0]
0x5F06	R_CTRL06	0x02	RW	Bit[7:0]: Manual window height[15:8]
0x5F07	R_CTRL07	0x08	RW	Bit[7:0]: Manual window height[7:0]
0x5F08	R_CTRL08	0x00	RW	Bit[2]: Flip offset enable Bit[1]: Mirror offset enable Bit[0]: Manual window setting enable
0x5F09~ 0x5F0C	RSVD	–	–	Reserved

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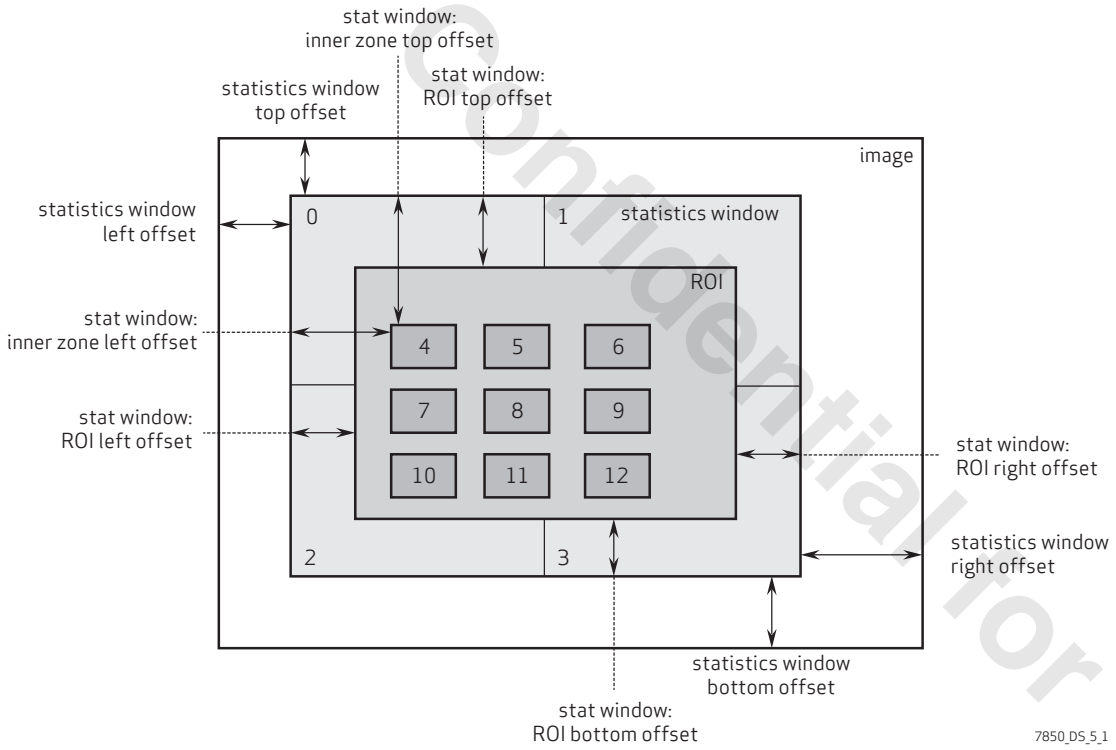
5 AEC/AGC algorithms

The AEC/AGC statistics are computed to determine which exposure/gain must be applied in the next frames. There are three different exposure channels in the OV7850, L for long exposure, S for short exposure and VS for very short exposure. For a three exposure working mode, L and S use almost the same algorithm to estimate the new exposure based on the weighted average of current exposure. The difference is that the L channel can change freely in the whole range, but the S channel is limited by the new expected dynamic range and new L. The VS channel keeps a fixed ratio to S channel. The AEC/AGC algorithm will decide whether the reference channels have the suitable brightness.

figure 5-1 statistics window diagram



A statistics window is given by registers {0x5A81[1:0], 0x5A82}, {0x5A83[1:0], 0x5A84}, {0x5A85[1:0], 0x5A86} and {0x5A87[1:0], 0x5A88} and defines how many rows/columns are excluded from left, top, right and bottom side. This window is common for both long, short and very short channels. The pixels outside are not included in the weighted average calculation.

In HDR mode, the dynamic range extension is dependent on the L, S, and VS channel exposure ratio. By default, the long and short exposure ratio is automatically adjusted according to the dynamic range of the scene and the target stable range. Short and very short ration is fixed, which can be changed by register 0x59BE/0x59BF. The OV7850 also supports fixed exposure ratio, which is enabled by register 0x5981[0]. The fixed exposure ratio is equal to the value of register

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0x599D. The exposure ratio here is not the ratio of exposure time, but also includes the sensitivity ratio which is calibrated by registers {0x59BC, 0x59BD}.

The statistics for AEC/AGC is calculated as a weighted average of a user defined range. The weighting of each pixel includes three parts:

- position weight (W_P)
- adaptive weight (combine weight) (W_C)
- luminance weight (W_Y)

5.1 position weight

The basic AEC/AGC algorithm determines whether the reference channels have the suitable brightness. To measure the brightness of the current frame, the pixels in the image are weighted by a position weight and a user-defined ROI weight.

The statistic window is evenly divided into four outer zones as shown in **figure 5-1**. The center portion of the statistic window is further divided evenly into nine inner zones. The top-left corner coordinate of the long channel 3x3 inner zones relative to the top-left corner of the statistic window is set by registers ({0x5A92, 0x5A93}, {0x5A94, 0x5A95}). The width and height of the L channel 3x3 inner zones are set by registers {0x5A96, 0x5A97}, {0x5A98, 0x5A99}, respectively. Similarly, the S channel top-left corner coordinate, width and height, are set by registers ({0x5A9A, 0x5A9B}, {0x5A9C, 0x5A9D}), and {0x5A9E, 0x5A9F}, {0x5AA0, 0x5AA1}, respectively.

The weight of L channel zones 0 through 12 are set by the 4 MSBs of 0x5AA2~0x5AAE. The weight of S channel zones 0 through 12 are set by the 4 LSBs of 0x5AA2~0x5AAE. The summation of the pixel value multiplied by the weight will be divided by the summation of the weight, so the weight is just a relative value.

A ROI window is defined to further differentiate the weight of inner and outer pixels. Registers {0x5AAF[1:0], 0x5AB0}, {0x5AB1[1:0], 0x5AB2}, {0x5AB3[1:0], 0x5AB4} and {0x5AB5[1:0], 0x5AB6} define the distance from the left, top, right and bottom side of the statistics window to the left, top, right and bottom side of the ROI window, respectively, for the L channel. Similarly, registers {0x5AB8[1:0], 0x5AB9}, {0x5ABA[1:0], 0x5ABB}, {0x5ABC[1:0], 0x5ABD} and {0x5ABE[1:0], 0x5ABF} define the S channel ROI position and size. Inside the ROI, the L channel weight is defined by the MSBs in register 0x5AB7 and outside the ROI, the L channel weight is defined by the LSBs in register 0x5AB7. Similarly, weight for the S channel is defined in register 0x5AC0. Same as zone weight, the ROI weight is also a relative value.

The pixel value is weighted by both zone weight and ROI weight.

$W_{POS} = W_{zone} \times W_{ROI}$

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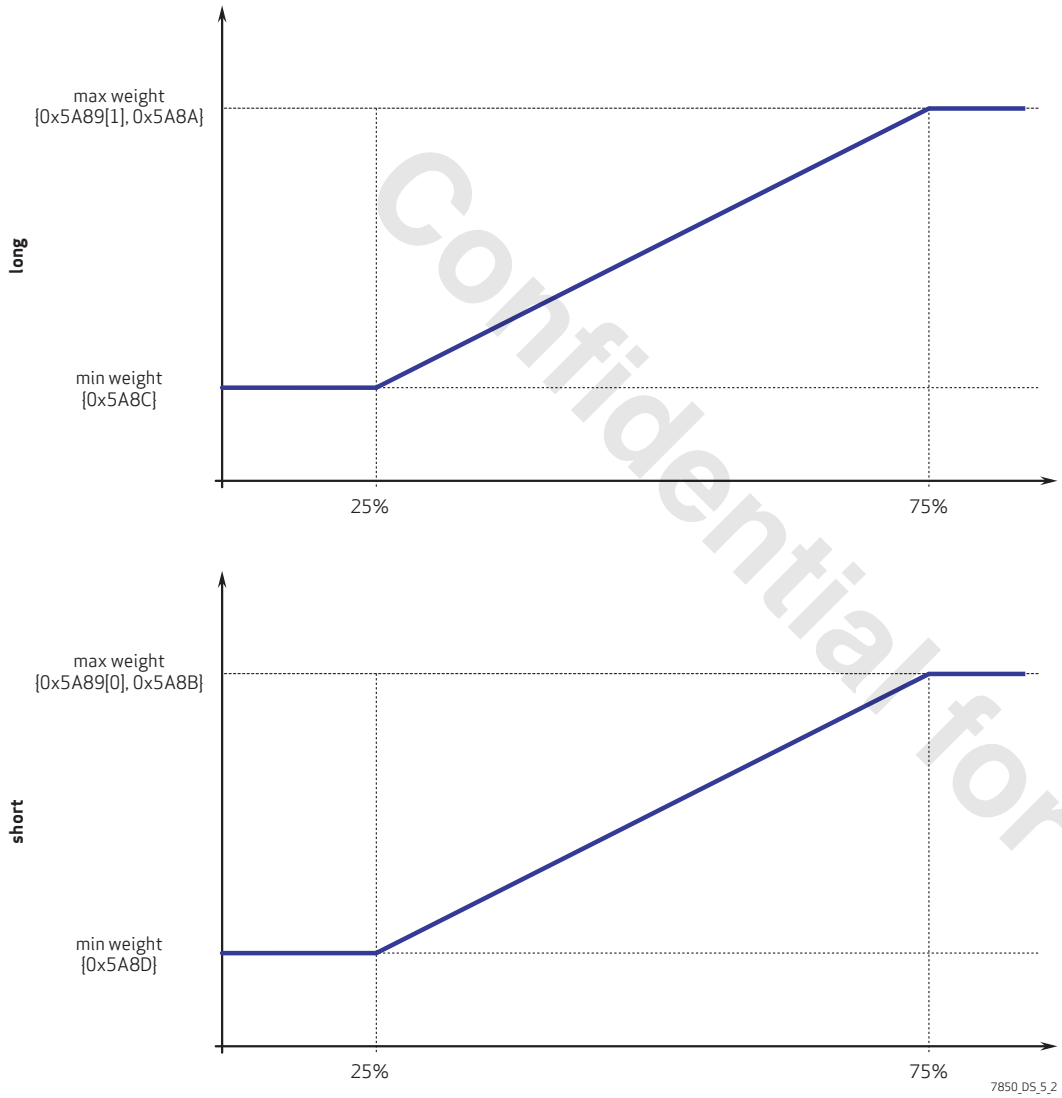
5.2 adaptive weight (combination weight)

The AEC/AGC weighs each pixel by $w_c(x,y)$ to calculate the average of long and short exposure image according to the combination weight $w_c(x,y)$, where c means long and short exposure.

figure 5-2 adaptive weight curve



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W_{min} – Register 0x5A8C for long and 0x5A8D for short

W_{max} – Register {0x5A89[1], 0x5A8A[7:0]} for long, and {0x5A89[0], 0x5A8B[7:0]} for short

5.3 luminance weight

To emphasize the dark or high light pixel in the average calculation, the weight is adaptive to pixel value and different channels put different emphasis to different light levels.

A weighted luminance summary and weight summary will be:

SumM = ∑(Y*W)

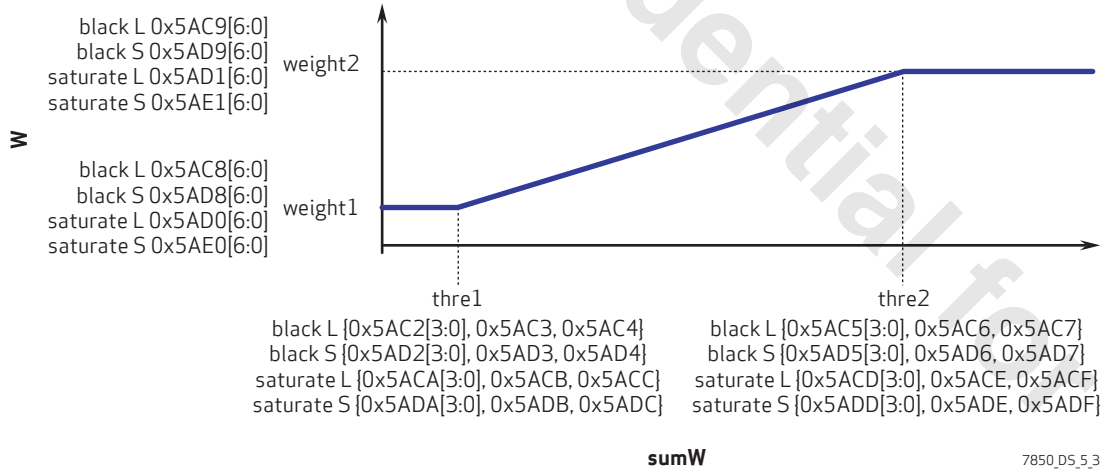
SumW = ∑(W)

- Y is the luminance of each pixel
- W is former calculated pixel weight (multiplication of combine weight and position weight).

Based on the level, the image will be classified into black (low light), middle tone and high light. Also, they receive the summary for each range respectively. The threshold for the pixels to be counted as black (low light threshold) and high light (high light threshold) is set by registers 0x5A90 and 0x5A91.

Luminance weight will be calculated based on the summary weights (SumW) of each luminance range respectively. For black (low light) and high light (saturate) range, weights are calculated as in **figure 5-3**.

figure 5-3 luminance threshold curve



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The luminance weight for middle tone is always 1 and the weight for the black and high light will depend on the number of black or high light pixels.

The latest weighted luminance average will be:

$$MeanY = ((SM_B \times W_{LB}) + SM_M + (SM_H \times W_{LH})) / ((SW_B \times W_{LB}) + SW_M + (SW_H \times WL_H))$$

- MeanY is the latest statistics result
- SM_B, W_{LB} and SW_B: identifiers for weight luminance summary, luminance weight and weight summary of black (low light) range pixels
- SM_M and SW_M: identifiers for weight luminance summary, weight summary of middle tone range pixels
- SM_H, W_{LH} and S_{WH}: identifiers for weight luminance summary, luminance weight and weight summary of high light (saturate) range pixels

The long channel is used to see the details in dark areas. By increasing the weight for dark pixels, AEC/AGC will tend to increase the exposure for shadows and result in more details in shadow area.

The short channel is used to see details in bright areas. By increasing the weight for high light pixels, AEC/AGC will tend to decrease the exposure for saturated areas, resulting in more details in bright areas.

For a three exposure working mode, L and S use almost the same algorithm for control, which estimates the new exposure based on the weighted average of current exposure. The difference is the long exposure can change freely in the whole range, but the short exposure is limited by the new expected dynamic range and the new long exposure. As for VS channel, it keeps a fixed ratio to S.

Considering the non-linearity of the weighted average, there are three regions based on the distance between current weighted average and the target: fast range, slow range and stable range. When the current weighted average changes within the stable range, the exposure will remain stable. The difference between slow range and fast range is the changing speed of exposure. In slow range, the exposure is limited to changing in small steps.

The AEC/AGC adjustment step is calculated from the distance between the current average value and the target. When the current weighted average is far from the stable range, a large adjustment step is applied to quickly bring the average value to stable range. Register 0x5997 defines the percentage of the adjustment with respect to the distance to the target value. The exposure adjustment is further limited by the ratio to the exposure time of the previous frame. The maximum current-to-previous-frame exposure ratio range is limited to the range of (16/0x599B, 0x599B/16).

When the current weighted average is close to the stable range, a small adjustment step is applied to avoid overshoot or undershoot. Register 0x5999 defines the percentage of the adjustment with respect to the distance to the target value. The exposure adjustment is further limited by the ratio to the exposure time of the previous frame. The maximum current-to-previous-frame exposure ratio range is limited to the range of (1 - 0x599C/16, 1+ 0x599C/16).

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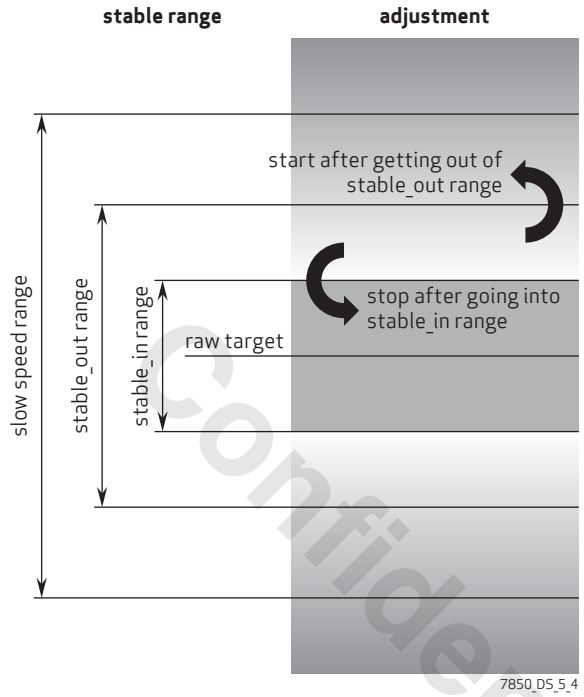
figure 5-4 automatic adjustment step mode diagram



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The OV7850 supports down sample statistics. A down scale rate can be set with register 0x5A8E[2:0]. Statistic type is also selectable between Y channel and the maximum data of R/G/B by register 0x5A80.

The OV7850 supports three different AEC/AGC stable range modes, AA, AB and ABC modes, defined by register bits 0x59C9[1:0]. In AA mode, all frames have the same AEC/AGC stable range. In AB mode, the AEC/AGC stable range of even and odd frames can be set to different values. ABC mode is the same as AB mode except that the frames split into three subsets and there are three different AEC/AGC targets. The exposure and gain of A, B and C frames are adjusted separately when register 0x5982 is set to 0. They can settle down to a slightly different value even with the same stable range. When register 0x5982 is set to 1, the exposure/gain of frame B and C is proportional to the exposure/gain of frame A. The exposure ratio between frame B and frame A is set by register 0x599F and the exposure ratio between frame C and A is set by register 0x59A0.

The exposure time and gain changes every two frames. At the end of the first frame, the new exposure time and gain will be estimated and the exposure time registers will be updated afterwards. The gain registers will be updated at the end of the second frame, so the third frame will have the new exposure time and gain.

The same algorithm is employed to adjust the exposure and gain for frame A, B and C in AB or ABC mode. The control register sets, however, are separated for frame A, B and C.

table 5-1 exposure time and gain

parameter	frame A	frame B	frame C
RAW target for long channel	0x598D	0x598E	0x598F
RAW target for short channel	0x5990	0x5991	0x5992
stable_in range	(RAW target - 0x5995, RAW target + 0x5995)		
stable_out range	(RAW target - 0x5996, RAW target + 0x5995)		
slow speed range for long channel	(RAW target for long channel - 0x5993, RAW target for long channel + 0x5993)		
slow speed range for short channel	(RAW target for long channel - 0x5994, RAW target for long channel + 0x5994)		
fast adjustment step for long channel	(0x5997/16) x (currentlevel - targetlevel)		
fast adjustment step for short channel	(0x0x5998/16) x (currentlevel - targetlevel)		
slow adjustment step for long channel	(0x5999/16) x (currentlevel - targetlevel)		
slow adjustment step for short channel	(0x599A/16)x (currentlevel - targetlevel)		
max fast current-to-previous-frame exposure ratio range	(16/0x599B, 0x599B/16)		
max slow current-to-previous frame exposure ratio range	(1 - 0x599C/16, 1 + 0x599C/16)		

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The user can also specify the target brightness of the final image output. The brightness target, however, does not affect AEC/AGC. The OV7850 adjusts the gamma curve and HDR gain to achieve the brightness target, but is not guaranteed to reach the target value. The tone mapping will change the image brightness afterwards.

In extremely dark situations, night mode is activated (0x5983), allowing the sensor to extend the frame period and, thus, the exposure time. The frame period can be extended a maximum of 3 times the original frame period (register 0x59C7). So, for the L channel, the maximum exposure time can be up to 4 times the original frame period. For S and VS channel, there are other controls which limit the maximum exposure time. Registers 0x59F0~0x5A01 show the maximum gain multiplied by the maximum exposure for each channel.

To avoid image banding under a flickering light source, the exposure time can be adjusted in steps of integer multiples of the light flickering period, enabled by registers 0x5986, 0x5987 and 0x5988 for L, S and VS channels. The light source flicker frequency (50/60 Hz) is selected by register 0x598C.

5.4 exposure modes

There are five sensor exposure modes supported in the ISP.

table 5-2 sensor exposure modes

exposure mode	valid data	description
three	L, S, VS	four HDR combine modes support
LS	L, S	combine L and S
LVS	L, VS	combine L and VS
long	L	output format can not be RAW20/18/16
traffic	L, S, VS	four HDR combine mode support restrict S to ensure capture LED light frequency

5.5 manual exposure mode

A backend processor can fully control the exposure/gain for both long and short exposure using the following sequence for AA mode:

1. Disable auto exposure 0x5000[7]=0
2. Enter manual mode by setting 0x59C9[0] = 1
3. Choose manual AEC AA mode 0x5502 = 0
4. Set exposure/gain using 0x59CC~0x59EF
5. Enable exposure/gain by 0x59CA = 2

Manual mode for AB and ABC modes is enabled by registers 0x59C9[1] and 0x59C9[2]. The manual exposure time for L, S and VS channels for frames A, B and C is set by registers 0x59CC~0x59E3. Gain is set by registers 0x59E4~0x59EF. After setting the exposure and gain, write 0x01 to register 0x59CA to apply them.

The OV7850 supports context switching with AEC/AGC target range, manual exposure, and gain.

In AB or ABC mode, manual mode is enabled by register 0xC309. The long and short channel exposure of frames A, B and C is set by registers 0x59CC~0x59E3, respectively. Gain is set by registers 0x59E4~0x59EF, respectively. After setting exposure and gain, write 0x01 to register 0x59CA to apply them. **figure 5-5** shows the detailed exposure latch diagram.

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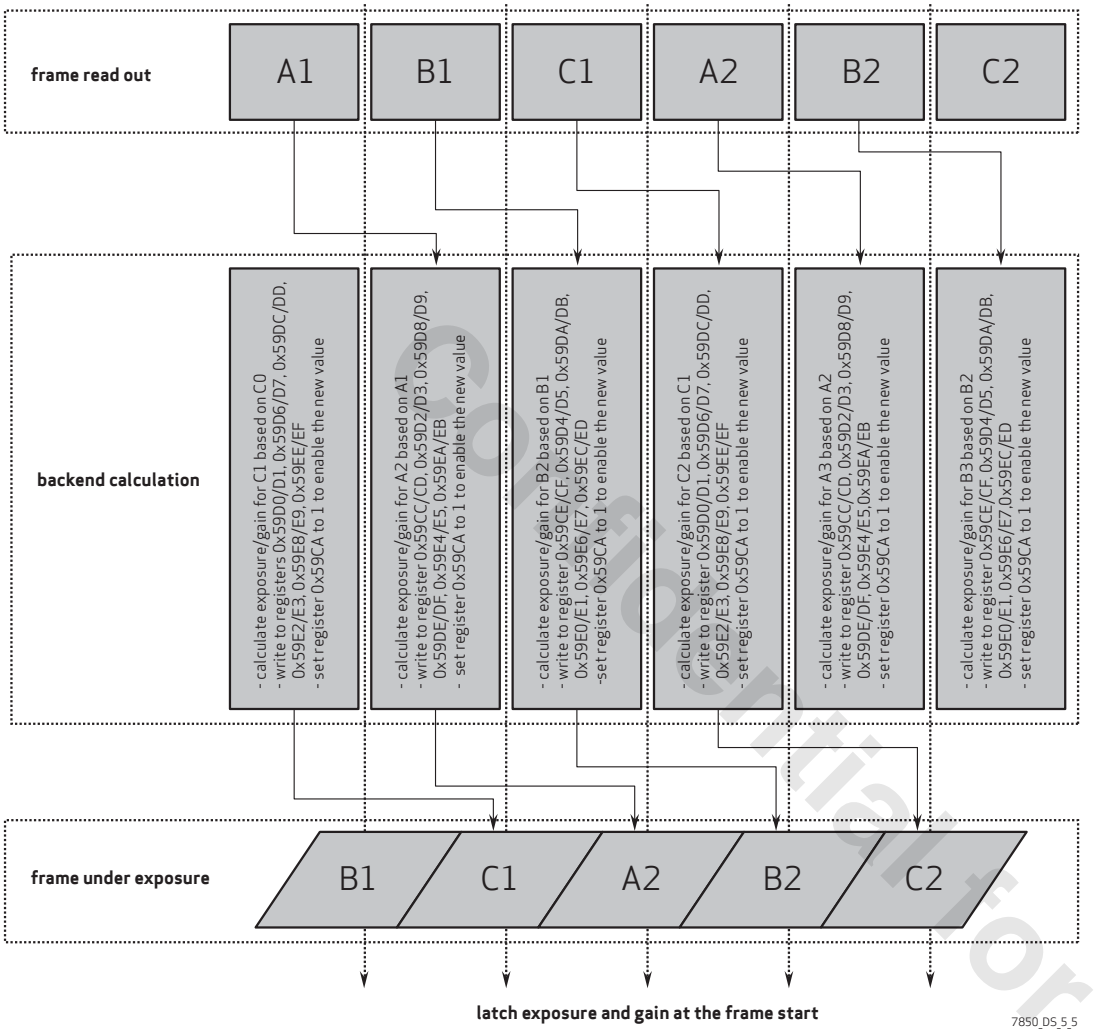
figure 5-5 ABC manual exposure mode diagram



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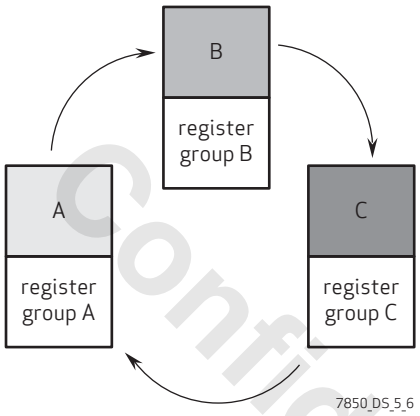
5.5.1 ABC context switch

In AB or ABC mode, the AEC/AGC target range, manual exposure, and gain can automatically switch frames A, B and C. A group of registers can also automatically switch frames A, B and C (see **figure 5-6** for more details). The registers set up the specific context (e.g., the output size and format) for frames A, B and C).

figure 5-6 context switching diagram



Other than the exposure/gain, the OV7850 supports automatic context switch between two/three groups of registers for AB or ABC frame, respectively

The context switch is implemented by the group register write.

- Set up the buffer for register groups 1, 2 and 3. The entry number of group 0 is set by register 0x3200. Group 1 is set by register 0x3201. Group 2 is set by 0x3202. Group 3 is set by register 0x3203. The total buffer size is 768 bytes by default, so it can program about 256 registers
- Record the register group for frame A, B, and C

```
60 3204 80; start record registers for group 0 / frame A
................
60 3204 00 ; finish record registers for group 0 / frame A

60 3204 84; start record register s for group 1 / frame B
................
60 3204 04 ; finish record registers for group 1 / frame B

60 3204 88; start record register s for group 2 / frame C
................
60 3204 08 ; finish record registers for group 2 / frame C
```

- Write 0x02 to register 0x3207 to launch the group write

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table 5-3 AEC control registers (sheet 1 of 7)

address	register name	default value	R/W	description
0x5980	MANUALCGENABLE	–	–	Manual Conversion Gain Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5981	FIXEDRATIOENABLE	–	–	Fixed ratio Between L and S Enable 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5982	GPMODEEN	–	–	Geometric Proportion Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5983	NIGHTMODE	–	–	Night Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5984	ONLYINSERTFRAMEEN	–	–	Only Insert Frame When in Night Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5985	HTBLCENABLE	–	–	High Temperature BLC Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.

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table 5-3 AEC control registers (sheet 2 of 7)

address	register name	default value	R/W	description
0x5986	BANDINGFILTERENABLE	–	–	Banding Filter 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5987	BANDINGFILTERSHORT ENABLE	–	–	Short Banding Filter 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5988	BANDINGFILTERVS ENABLE	–	–	VS Banding Filter 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x5989	LESSTHAN1BANDENABLE	–	–	Less Than One Band Exposure Mode 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x598A	LESSTHAN1BANDSHORT ENABLE	–	–	Less Than One Band Exposure for Short 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x598B	LESSTHAN1BANDVS ENABLE	–	–	Less Than One Band Exposure for VS 0: Disable 1: Enable When register value is 0x00, it means function is disabled; all other values mean function is enabled. Default value is random.
0x598C	BANDINGFILTERFLAG	–	–	Light Source Type 00: Frequency is zero or very high 01: 60Hz 10: 50Hz

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table 5-3 AEC control registers (sheet 3 of 7)

address	register name	default value	R/W	description
0x598D	TARGETY_0_0	–	–	Target of RAW Data for Long 0
0x598E	TARGETY_0_1	–	–	Target of RAW Data for Long 1
0x598F	TARGETY_0_2	–	–	Target of RAW Data for Long 2
0x5990	TARGETY_1_0	–	–	Target of RAW Data for Short 0
0x5991	TARGETY_1_1	–	–	Target of RAW Data for Short 1
0x5992	TARGETY_1_2	–	–	Target of RAW Data for Short 2
0x5993	SLOWRANGE_0	–	–	Slow Range for Long
0x5994	SLOWRANGE_1	–	–	Slow Range for Short
0x5995	STABLERANGE_0	–	–	Range Become Stable from Unstable
0x5996	STABLERANGE_1	–	–	Range Become Unstable from Stable
0x5997	FASTSTEP_0	–	–	Fast AEC Adjustment Step for Long
0x5998	FASTSTEP_1	–	–	Fast AEC Adjustment Step for Short
0x5999	SLOWSTEP_0	–	–	Slow AEC Adjustment Step for Long
0x599A	SLOWSTEP_1	–	–	Slow AEC Adjustment Step for Short
0x599B	MAXFASTRATIO	–	–	Max Fast Adjustment Ratio
0x599C	MAXSLOWRATIO	–	–	Max Slow Adjustment Ratio
0x599D	LSFIXEDRATIO	–	–	Fixed Ratio Between L and S
0x599E	NIGHTMODESTEP	–	–	AEC Adjustment Step in Night Mode
0x599F	GPMODERATIO_0	–	–	B/A Ratio in GP Mode
0x59A0	GPMODERATIO_1	–	–	C/A Ratio in GP Mode
0x59A1	EXPRATIOSTEP	–	–	L/S Ratio Change Step
0x59A2	NONHDRSTEP	–	–	L/S Change Step in Non-HDR Mode
0x59A3	PRECHARGEWIDTH	–	–	Pre Charge Width
0x59A4	MAXCAMERAGAIN_0_H	–	–	Bit[2:0]: Max gain for long[10:8]
0x59A5	MAXCAMERAGAIN_0_L	–	–	Bit[7:0]: Max gain for long[7:0]
0x59A6	MAXCAMERAGAIN_1_H	–	–	Bit[1:0]: Max gain for short[9:8]
0x59A7	MAXCAMERAGAIN_1_L	–	–	Bit[7:0]: Max gain for short[7:0]
0x59A8	MAXCAMERAGAIN_2_H	–	–	Bit[1:0]: Max gain for VS[9:8]
0x59A9	MAXCAMERAGAIN_2_L	–	–	Bit[7:0]: Max gain for VS[7:0]
0x59AA	MINCAMERAGAIN_0_H	–	–	Bit[1:0]: Min gain for long[9:8]

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table 5-3 AEC control registers (sheet 4 of 7)

address	register name	default value	R/W	description
0x59AB	MINCAMERAGAIN_0_L	–	–	Bit[7:0]: Min gain for long[7:0]
0x59AC	MINCAMERAGAIN_1_H	–	–	Bit[1:0]: Min gain for short[9:8]
0x59AD	MINCAMERAGAIN_1_L	–	–	Bit[7:0]: Min gain for short[7:0]
0x59AE	MINCAMERAGAIN_2_H	–	–	Bit[1:0]: Min gain for VS[9:8]
0x59AF	MINCAMERAGAIN_2_L	–	–	Bit[7:0]: Min gain for VS[7:0]
0x59B0	MAXEXPOSURE_0_H	–	–	Bit[7:0]: Max exposure for long[15:8]
0x59B1	MAXEXPOSURE_0_L	–	–	Bit[7:0]: Max exposure for long[7:0]
0x59B2	MAXEXPOSURE_1_H	–	–	Bit[7:0]: Max exposure for short[15:8]
0x59B3	MAXEXPOSURE_1_L	–	–	Bit[7:0]: Max exposure for short[7:0]
0x59B4	MAXEXPOSURE_2_H	–	–	Bit[7:0]: Max exposure for VS[15:8]
0x59B5	MAXEXPOSURE_2_L	–	–	Bit[7:0]: Max exposure for VS[7:0]
0x59B6	MINEXPOSURE_0_H	–	–	Bit[7:0]: Min exposure for long[15:8]
0x59B7	MINEXPOSURE_0_L	–	–	Bit[7:0]: Min exposure for long[7:0]
0x59B8	MINEXPOSURE_1_H	–	–	Bit[7:0]: Min exposure for short[15:8]
0x59B9	MINEXPOSURE_1_L	–	–	Bit[7:0]: Min exposure for short[7:0]
0x59BA	MINEXPOSURE_2_H	–	–	Bit[7:0]: Min exposure for VS[15:8]
0x59BB	MINEXPOSURE_2_L	–	–	Bit[7:0]: Min exposure for VS[7:0]
0x59BC	LSSENSITIVITYRATIO_H	–	–	Bit[7:0]: L/S sensitivity ratio[15:8]
0x59BD	LSSENSITIVITYRATIO_L	–	–	Bit[7:0]: L/S sensitivity ratio[7:0]
0x59BE	SVSFIXEDRATIO_H	–	–	Bit[7:0]: S/VS exposure ratio[15:8]
0x59BF	SVSFIXEDRATIO_L	–	–	Bit[7:0]: S/VS exposure ratio[7:0]
0x59C0	BANDVALUE60HZ_H	–	–	Bit[7:0]: Band filter value for 60Hz[15:8]
0x59C1	BANDVALUE60HZ_L	–	–	Bit[7:0]: Band filter value for 60Hz[7:0]
0x59C2	BANDVALUE50HZ_H	–	–	Bit[7:0]: Band filter value for 50Hz[15:8]
0x59C3	BANDVALUE50HZ_L	–	–	Bit[7:0]: Band filter value for 50Hz[7:0]
0x59C4	MAXRATIO_H	–	–	Bit[7:0]: Max L/S ratio[15:8]
0x59C5	MAXRATIO_L	–	–	Bit[7:0]: Max L/S ratio[7:0]
0x59C6	MINRATIO	–	–	Min L/S Ratio
0x59C7	MAXINSERTFRAME	–	–	Maximum Insert Frames at Night Mode

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table 5-3 AEC control registers (sheet 5 of 7)

address	register name	default value	R/W	description
0x59C8	NVTSWRITEMODE	–	–	VTS Write Mode 0: Write with exposure 1: Write with gain
0x59C9	AECMANUALMODE	–	–	Manual AEC A/B/C Mode Selected 00: AA mode 01: AB mode 10: ABC mode
0x59CA	AECMANUALDONE	–	–	Manual AEC Start Mode 00: Inactive 01: Active 10: Always active
0x59CB	ALLOWFRACTALEXP	–	–	Allow Fractal Resolution for VS Exposure
0x59CC	AECMANUALEXP_0_0_H	–	–	Bit[7:0]: Manual exposure for 0 for long[15:8]
0x59CD	AECMANUALEXP_0_0_L	–	–	Bit[7:0]: Manual exposure for 0 for long[7:0]
0x59CE	AECMANUALEXP_0_1_H	–	–	Bit[7:0]: Manual exposure for 1 for long[15:8]
0x59CF	AECMANUALEXP_0_1_L	–	–	Bit[7:0]: Manual exposure for 1 for long[7:0]
0x59D0	AECMANUALEXP_0_2_H	–	–	Bit[7:0]: Manual exposure for 2 for long[15:8]
0x59D1	AECMANUALEXP_0_2_L	–	–	Bit[7:0]: Manual exposure for 2 for long[7:0]
0x59D2	AECMANUALEXP_1_0_H	–	–	Bit[7:0]: Manual exposure for 0 for short[15:8]
0x59D3	AECMANUALEXP_1_0_L	–	–	Bit[7:0]: Manual exposure for 0 for short[7:0]
0x59D4	ECMANUALEXP_1_1_H	–	–	Bit[7:0]: Manual exposure for 1 for short[15:8]
0x59D5	AECMANUALEXP_1_1_L	–	–	Bit[7:0]: Manual exposure for 1 for short[7:0]
0x59D6	AECMANUALEXP_1_2_H	–	–	Bit[7:0]: Manual exposure for 2 for short[15:8]
0x59D7	AECMANUALEXP_1_2_L	–	–	Bit[7:0]: Manual exposure for 2 for short[7:0]
0x59D8	AECMANUALEXP_2_0_H	–	–	Bit[7:0]: Manual exposure for 0 for VS[15:8]

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table 5-3 AEC control registers (sheet 6 of 7)

address	register name	default value	R/W	description
0x59D9	AECMANUALEXP_2_0_L	–	–	Bit[7:0]: Manual exposure for 0 for VS[7:0]
0x59DA	AECMANUALEXP_2_1_H	–	–	Bit[7:0]: Manual exposure for 1 for VS[15:8]
0x59DB	AECMANUALEXP_2_1_L	–	–	Bit[7:0]: Manual exposure for 1 for VS[7:0]
0x59DC	AECMANUALEXP_2_2_H	–	–	Bit[7:0]: Manual exposure for 2 for VS[15:8]
0x59DD	AECMANUALEXP_2_2_L	–	–	Bit[7:0]: Manual exposure for 2 for VS[7:0]
0x59DE	AECMANUALGAIN_0_0_H	–	–	Bit[7:0]: Manual gain for 0 for long[15:8]
0x59DF	AECMANUALGAIN_0_0_L	–	–	Bit[7:0]: Manual gain for 0 for long[7:0]
0x59E0	AECMANUALGAIN_0_1_H	–	–	Bit[7:0]: Manual gain for 1 for long[15:8]
0x59E1	AECMANUALGAIN_0_1_L	–	–	Bit[7:0]: Manual gain for 1 for long[7:0]
0x59E2	AECMANUALGAIN_0_2_H	–	–	Bit[7:0]: Manual gain for 2 for long[15:8]
0x59E3	AECMANUALGAIN_0_2_L	–	–	Bit[7:0]: Manual gain for 2 for long[7:0]
0x59E4	AECMANUALGAIN_1_0_H	–	–	Bit[7:0]: Manual gain for 0 for short[15:8]
0x59E5	AECMANUALGAIN_1_0_L	–	–	Bit[7:0]: Manual gain for 0 for short[7:0]
0x59E6	AECMANUALGAIN_1_1_H	–	–	Bit[7:0]: Manual gain for 1 for short[15:8]
0x59E7	AECMANUALGAIN_1_1_L	–	–	Bit[7:0]: Manual gain for 1 for short[7:0]
0x59E8	AECMANUALGAIN_1_2_H	–	–	Bit[7:0]: Manual gain for 2 for short[15:8]
0x59E9	AECMANUALGAIN_1_2_L	–	–	Bit[7:0]: Manual gain for 2 for short[7:0]
0x59EA	AECMANUALGAIN_2_0_H	–	–	Bit[7:0]: Manual gain for 0 for VS[15:8]
0x59EB	AECMANUALGAIN_2_0_L	–	–	Bit[7:0]: Manual gain for 0 for VS[7:0]
0x59EC	AECMANUALGAIN_2_1_H	–	–	Bit[7:0]: Manual gain for 1 for VS[15:8]
0x59ED	AECMANUALGAIN_2_1_L	–	–	Bit[7:0]: Manual gain for 1 for VS[7:0]
0x59EE	AECMANUALGAIN_2_2_H	–	–	Bit[7:0]: Manual gain for 2 for VS[15:8]
0x59EF	AECMANUALGAIN_2_2_L	–	–	Bit[7:0]: Manual gain for 2 for VS[7:0]
0x59F0	MAXTOTALEXP_0_BYTE0	–	–	Bit[7:0]: Max total exposure for long[31:24]
0x59F1	MAXTOTALEXP_0_BYTE1	–	–	Bit[7:0]: Max total exposure for long[23:16]
0x59F2	MAXTOTALEXP_0_BYTE2	–	–	Bit[7:0]: Max total exposure for long[15:8]
0x59F3	MAXTOTALEXP_0_BYTE3	–	–	Bit[7:0]: Max total exposure for long[7:0]

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table 5-3 AEC control registers (sheet 7 of 7)

address	register name	default value	R/W	description
0x59F4	MAXTOTALEXP_1_BYTE0	–	–	Bit[7:0]: Max total exposure for short[31:24]
0x59F5	MAXTOTALEXP_1_BYTE1	–	–	Bit[7:0]: Max total exposure for short[23:16]
0x59F6	MAXTOTALEXP_1_BYTE2	–	–	Bit[7:0]: Max total exposure for short[15:8]
0x59F7	MAXTOTALEXP_1_BYTE3	–	–	Bit[7:0]: Max total exposure for short[7:0]
0x59F8	MAXTOTALEXP_2_BYTE0	–	–	Bit[7:0]: Max total exposure for VS[31:24]
0x59F9	MAXTOTALEXP_2_BYTE1	–	–	Bit[7:0]: Max total exposure for VS[23:16]
0x59FA	MAXTOTALEXP_2_BYTE2	–	–	Bit[7:0]: Max total exposure for VS[15:8]
0x59FB	MAXTOTALEXP_2_BYTE3	–	–	Bit[7:0]: Max total exposure for VS[7:0]
0x59FC	MINTOTALEXP_0_H	–	–	Bit[7:0]: Min total exposure for long[15:8]
0x59FD	MINTOTALEXP_0_L	–	–	Bit[7:0]: Min total exposure for long[7:0]
0x59FE	MINTOTALEXP_1_H	–	–	Bit[7:0]: Min total exposure for short[15:8]
0x59FF	MINTOTALEXP_1_L	–	–	Bit[7:0]: Min total exposure for short[7:0]
0x5A00	MINTOTALEXP_2_H	–	–	Bit[7:0]: Min total exposure for VS[15:8]
0x5A01	MINTOTALEXP_2_L	–	–	Bit[7:0]: Min total exposure for VS[7:0]
0x5A02	MANUALCG	–	–	Manual Conversion Gain Value
0x5A03	HIGHCONVERSIONG	–	–	High Conversion Gain Value This register value must be initialized by user and must not be removed from start up sequence. Default value is random.
0x5A04	CGTH0	–	–	Conversion Gain Switch Th0
0x5A05	CGTh1	–	–	Conversion Gain Switch Th1
0x5A06	BLCTRIGTEMPTHRE	–	–	BLC Temperature Difference Trigger Threshold
0x5A07	BLCOFFSETDACTH0	–	–	High Temperature BLC Offset Threshold 0
0x5A08	BLCOFFSETDACTH1	–	–	High Temperature BLC Offset Threshold 1
0x5A09~ 0x5A3F	RSVD	–	–	Reserved

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table 5-4 AEC_AGC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5A80	R_AEC_AGC_STAT_TYPE	0x00	RW	Bit[0]: AECAGC statistic type 0: Y channel 1: Max (R, G, B)
0x5A81	R_STAT_WIN_LEFT_H	0x00	RW	Bit[1:0]: Statistic window left offset[9:8]
0x5A82	R_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Statistic window left offset[7:0]
0x5A83	R_STAT_WIN_RIGHT_H	0x00	RW	Bit[1:0]: Statistic window right offset[9:8]
0x5A84	R_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Statistic window right offset[7:0]
0x5A85	R_STAT_WIN_TOP_H	0x00	RW	Bit[1:0]: Statistic window top offset[9:8]
0x5A86	R_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Statistic window top offset[7:0]
0x5A87	R_STAT_WIN_BOTTOM_H	0x00	RW	Bit[1:0]: Statistic window bottom offset[9:8]
0x5A88	R_STAT_WIN_BOTTOM_L	0x0A	RW	Bit[7:0]: Statistic window bottom offset[7:0]
0x5A89	R_MAX_W_H	0x01	RW	Bit[1]: MaxW[0] Bit[0]: MaxW[1]
0x5A8A	R_MAX_W_0_L	0x20	RW	Bit[7:0]: Max W[0]
0x5A8B	R_MAX_W_1_L	0x00	RW	Bit[7:0]: Max W[1]
0x5A8C	R_MIN_W_0	0x01	RW	Bit[7:0]: Min W[0]
0x5A8D	R_MIN_W_1	0x01	RW	Bit[7:0]: Min W[1]
0x5A8E	R_STAT_DS_RATE	0x04	RW	Bit[2:0]: State down sample rate
0x5A8F	R_POS_W_SHIFT	0x00	RW	Bit[1:0]: PosW shift
0x5A90	R_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Threshold to define low light statistics
0x5A91	R_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Threshold to define high light statistics
0x5A92	R_WIN_LEFT_0_H	0x00	RW	Bit[1:0]: Win left[0][9:8]
0x5A93	R_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Win left[0][7:0]
0x5A94	R_WIN_TOP_0_H	0x00	RW	Bit[1:0]: Win top[0][9:8]
0x5A95	R_WIN_TOP_0_L	0x60	RW	Bit[7:0]: Win top[0][7:0]
0x5A96	R_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[1:0]: Stat win width[0][9:8]
0x5A97	R_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Stat win width[0][7:0]
0x5A98	R_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[1:0]: Stat win height[0][9:8]

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table 5-4 AEC_AGC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5A99	R_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Stat win height[0][7:0]
0x5A9A	R_WIN_LEFT_1_H	0x00	RW	Bit[1:0]: Win left[1][9:8]
0x5A9B	R_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Win left[1][7:0]
0x5A9C	R_WIN_TOP_1_H	0x00	RW	Bit[1:0]: Win top[1][9:8]
0x5A9D	R_WIN_TOP_1_L	0x60	RW	Bit[7:0]: Win top[1][7:0]
0x5A9E	R_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[1:0]: Stat win width[1][9:8]
0x5A9F	R_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Stat win width[1][7:0]
0x5AA0	R_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[1:0]: Stat win height[1][9:8]
0x5AA1	R_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Stat win height[1][7:0]
0x5AA2	R_WEIGHTS_0	0x11	RW	Bit[7:4]: Weights[0][0] Bit[3:0]: Weights[1][0]
0x5AA3	R_WEIGHTS_1	0x11	RW	Bit[7:4]: Weights[0][1] Bit[3:0]: Weights[1][1]
0x5AA4	R_WEIGHTS_2	0x11	RW	Bit[7:4]: Weights[0][2] Bit[3:0]: Weights[1][2]
0x5AA5	R_WEIGHTS_3	0x11	RW	Bit[7:4]: Weights[0][3] Bit[3:0]: Weights[1][3]
0x5AA6	R_WEIGHTS_4	0x11	RW	Bit[7:4]: Weights[0][4] Bit[3:0]: Weights[1][4]
0x5AA7	R_WEIGHTS_5	0x11	RW	Bit[7:4]: Weights[0][5] Bit[3:0]: Weights[1][5]
0x5AA8	R_WEIGHTS_6	0x11	RW	Bit[7:4]: Weights[0][6] Bit[3:0]: Weights[1][6]
0x5AA9	R_WEIGHTS_7	0x11	RW	Bit[7:4]: Weights[0][7] Bit[3:0]: Weights[1][7]
0x5AAA	R_WEIGHTS_8	0x11	RW	Bit[7:4]: Weights[0][8] Bit[3:0]: Weights[1][8]
0x5AAB	R_WEIGHTS_9	0x11	RW	Bit[7:4]: Weights[0][9] Bit[3:0]: Weights[1][9]
0x5AAC	R_WEIGHTS_10	0x11	RW	Bit[7:4]: Weights[0][10] Bit[3:0]: Weights[1][10]
0x5AAD	R_WEIGHTS_11	0x11	RW	Bit[7:4]: Weights[0][11] Bit[3:0]: Weights[1][11]
0x5AAE	R_WEIGHTS_12	0x11	RW	Bit[7:4]: Weights[0][12] Bit[3:0]: Weights[1][12]

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table 5-4 AEC_AGC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5AAF	R_ROI_LEFT_0_H	0x00	RW	Bit[1:0]: ROI left[0][9:8]
0x5AB0	R_ROI_LEFT_0_L	0x00	RW	Bit[7:0]: ROI left[0][7:0]
0x5AB1	R_ROI_TOP_0_H	0x00	RW	Bit[1:0]: ROI top[0][9:8]
0x5AB2	R_ROI_TOP_0_L	0x00	RW	Bit[7:0]: ROI top[0][7:0]
0x5AB3	R_ROI_RIGHT_0_H	0x00	RW	Bit[1:0]: ROI right[0][9:8]
0x5AB4	R_ROI_RIGHT_0_L	0x00	RW	Bit[7:0]: ROI right[0][7:0]
0x5AB5	R_ROI_BOTTOM_0_H	0x00	RW	Bit[1:0]: ROI bottom[0][9:8]
0x5AB6	R_ROI_BOTTOM_0_L	0x00	RW	Bit[7:0]: ROI bottom[0][7:0]
0x5AB7	R_ROI_WEIGHTS_0	0x11	RW	Bit[7:4]: ROI weights[0][0] Bit[3:0]: ROI weights[0][1]
0x5AB8	R_ROI_LEFT_1_H	0x00	RW	Bit[1:0]: ROI left[1][9:8]
0x5AB9	R_ROI_LEFT_1_L	0x00	RW	Bit[7:0]: ROI left[1][7:0]
0x5ABA	R_ROI_TOP_1_H	0x00	RW	Bit[1:0]: ROI top[1][9:8]
0x5ABB	R_ROI_TOP_1_L	0x00	RW	Bit[7:0]: ROI top[1][7:0]
0x5ABC	R_ROI_RIGHT_1_H	0x00	RW	Bit[1:0]: ROI right[1][9:8]
0x5ABD	R_ROI_RIGHT_1_L	0x00	RW	Bit[7:0]: ROI right[1][7:0]
0x5ABE	R_ROI_BOTTOM_1_H	0x00	RW	Bit[1:0]: ROI bottom[1][9:8]
0x5ABF	R_ROI_BOTTOM_1_L	0x00	RW	Bit[7:0]: ROI bottom[1][7:0]
0x5AC0	R_ROI_WEIGHTS_1	0x11	RW	Bit[7:4]: ROI weights[1][0] Bit[3:0]: ROI weights[1][1]
0x5AC1	R_ROI_SHIFT	0x00	RW	Bit[3:2]: ROI shift[0] Bit[1:0]: ROI shift[1]
0x5AC2	R_BLACK_THRE1_0_B2	0x00	RW	Bit[3:0]: Black threshold1[0] byte 2
0x5AC3	R_BLACK_THRE1_0_B1	0x01	RW	Bit[7:0]: Black threshold1[0] byte 1
0x5AC4	R_BLACK_THRE1_0_B0	0x00	RW	Bit[7:0]: Black threshold1[0] byte 0
0x5AC5	R_BLACK_THRE2_0_B2	0x00	RW	Bit[3:0]: Black threshold2[0] byte 2
0x5AC6	R_BLACK_THRE2_0_B1	0x08	RW	Bit[7:0]: Black threshold2[0] byte 1
0x5AC7	R_BLACK_THRE2_0_B0	0x00	RW	Bit[7:0]: Black threshold2[0] byte 0
0x5AC8	R_BLACK_WEIGHT1_0	0x10	RW	Bit[6:0]: Black weight1[0]
0x5AC9	R_BLACK_WEIGHT2_0	0x14	RW	Bit[6:0]: Black weight2[0]
0x5ACA	R_SATURATE_THRE1_0_B2	0x00	RW	Bit[3:0]: Saturate threshold1[0] byte 2

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table 5-4 AEC_AGC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5ACB	R_SATURATE_THRE1_0_B1	0x02	RW	Bit[7:0]: Saturate threshold1[0] byte 1
0x5ACC	R_SATURATE_THRE1_0_B0	0x00	RW	Bit[7:0]: Saturate threshold1[0] byte 0
0x5ACD	R_SATURATE_THRE2_0_B2	0x00	RW	Bit[3:0]: Saturate threshold2[0] byte 2
0x5ACE	R_SATURATE_THRE2_0_B1	0x04	RW	Bit[7:0]: Saturate threshold2[0] byte 1
0x5ACF	R_SATURATE_THRE2_0_B0	0x00	RW	Bit[7:0]: Saturate threshold2[0] byte 0
0x5AD0	R_SATURATE_WEIGHT1_0	0x08	RW	Bit[6:0]: Saturate weight1[0]
0x5AD1	R_SATURATE_WEIGHT2_0	0x12	RW	Bit[6:0]: Saturate weight2[0]
0x5AD2	R_BLACK_THRE1_1_B2	0x00	RW	Bit[3:0]: Black threshold1[1] byte 2
0x5AD3	R_BLACK_THRE1_1_B1	0x04	RW	Bit[7:0]: Black threshold1[1] byte 1
0x5AD4	R_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Black threshold1[1] byte 0
0x5AD5	R_BLACK_THRE2_1_B2	0x00	RW	Bit[3:0]: Black threshold2[1] byte 2
0x5AD6	R_BLACK_THRE2_1_B1	0x10	RW	Bit[7:0]: Black threshold2[1] byte 1
0x5AD7	R_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Black threshold2[1] byte 0
0x5AD8	R_BLACK_WEIGHT1_1	0x08	RW	Bit[6:0]: Black weight1[1]
0x5AD9	R_BLACK_WEIGHT2_1	0x12	RW	Bit[6:0]: Black weight2[1]
0x5ADA	R_SATURATE_THRE1_1_B2	0x00	RW	Bit[3:0]: Saturate threshold1[1] byte 2
0x5ADB	R_SATURATE_THRE1_1_B1	0x01	RW	Bit[7:0]: Saturate threshold1[1] byte 1
0x5ADC	R_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Saturate threshold1[1] byte 0
0x5ADD	R_SATURATE_THRE2_1_B2	0x00	RW	Bit[3:0]: Saturate threshold2[1] byte 2
0x5ADE	R_SATURATE_THRE2_1_B1	0x08	RW	Bit[7:0]: Saturate threshold2[1] byte 1
0x5ADF	R_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Saturate threshold2[1] byte 0
0x5AE0	R_SATURATE_WEIGHT1_1	0x10	RW	Bit[6:0]: Saturate weight1[1]
0x5AE1	R_SATURATE_WEIGHT2_1	0x14	RW	Bit[6:0]: Saturate weight2[1]
0x5AE2	R_MEAN_Y_0	–	R	Bit[7:0]: Mean Y[0]
0x5AE3	R_MEAN_Y_1	–	R	Bit[7:0] Mean Y[1]

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6 image output interface

The video stream from the output interface (see **figure 6-1**) is transmitted unprocessed (RAW 8/10) from the senor core or processed (YUV, RAW) from the ISP. The video data is formatted and output through the DVP or through the analog NTSC interface.

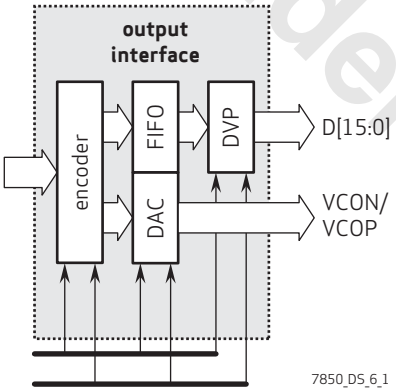
The FIFO adapts the internal clock speed to the DVP output speed and will start to read the FIFO after buffering enough data.

The TV DAC performs the digital-to-analog conversion of the NTSC video signal. The differential CVBS video signal from the DAC can be used to transmit to an analog NTSC capable display over long distances.

The sensor powers up to output analog NTSC (TV mode) by default. To enable video streaming, set register 0x303E[0] = 1.

A software reset is required to reset all registers back to their default values 0x303F[0] and the sensor will be in standby mode after the software reset. It is highly recommended to wait 10ms before programming other registers after a software reset.

figure 6-1 output interface diagram



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6.1 frame control

The frame control is located after the ISP block and selectively outputs or masks out certain frames. This function is enabled by default (0x4200[1]) to output all frames. The number of frames to mask out frame_off_number is set by register 0x4202[3:0] and the number of frames to send out, frame_on_number is set by register 0x4201[3:0]. The number of frames to output is summarized in **table 6-1**.

table 6-1 number of frames to output

output	frame_on_number	frame_off_number
frame control block repeats to mask out frame_off_number frames and then outputs frame_on_number frames	≠0x0	≠0x0
all frames will be masked	= 0x0	= 0xF
all frames will be sent out	= 0x0	= 0x0
frame control block will block frame_off_number frames and then send out all subsequent frames	= 0x0	0x0< > 0xF
frame control blocks output frame_on_number frames and then blocks all subsequent frames	>0x0	= 0x0

The frame control block will re-trigger when frame_on_number or frame_off_number changes.

The common usage of frame control is to mask out the first few frames when video streaming turns on, so frame_off_number and frame_on_number should be configured before video streaming is turned on.

table 6-2 frame control registers

address	register name	default value	R/W	description
0x4200	FCNT_CTRL	0x00	RW	Bit[3]: Reserved Bit[2]: Fcnt EOF select Bit[1]: Fcnt mask disable Bit[0]: Fcnt reset
0x4201	FRAME_ON_NUMBER	0x00	RW	Bit[3:0]: Frame on number
0x4202	FRAME_OFF_NUMBER	0x00	RW	Bit[3:0]: Frame off number
0x4203	MASK_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Rblue mask disable Bit[5]: Data mask disable Bit[4]: Valid mask disable Bit[3]: HREF mask disable Bit[2]: EOF mask disable Bit[1]: SOF mask disable Bit[0]: All mask disable

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6.2 digital video port

The digital video port (DVP) provides a 16-bit parallel data output for the supported formats in **table 6-3**. The data bit arrangement on the DVP output is a default arrangement and can be rearranged through registers, 0x470C[5] and 0x470B[6:4].

table 6-3 output format

format	description	data bit arrangement		DVP output
RAW 8	select one 8-bit RAW data from data1, data2, or data3[a]	data[7:0]		D[15:8]
RAW 10	select one 10-bit RAW data from data1, data2, or data3	data[9:0]		D[15:6]
RAW 8 x 2	select two 8-bit RAW data from data1, data2, or data3	cycle 1:	data1[7:0]	D[15:8]
		cycle 2:	data2[7:0]	D[15:8]
RAW 10 x 2	select two 10-bit RAW data from data1, data2, or data3	cycle 1:	data1[9:0]	D[15:6]
		cycle 2:	data2[9:0]	D[15:6]
RAW 8 x 3	data1, data2, and data3	cycle 1:	{data1[7:0],data2[7:0]}	D[15:0]
		cycle 2:	{data2[7:0],data3[7:0]}	D[15:0]
RAW 10 x 3	data1, data2, and data3	cycle 1:	{data1[9:0],data3[9:4]}	D[15:0]
		cycle 2:	{data2[9:0],data3[5:0]}	D[15:0]
	RAW 10 x 3 alternative configuration	cycle 1:	{data1[9:0],data2[9:4]}	D[15:0]
		cycle 2:	{data2[3:0],data3[9:0]}	D[15:2]
RAW 16	16-bit RAW format output (HDR combined)			D[15:0]
RAW 18	18-bit RAW format output (HDR combined)	cycle 1:	data[17:2]	D[15:0]
		cycle 2:	{data[9:0],data[5:0]}	
RAW 20	20-bit RAW format output (HDR combined)	cycle 1:	data[19:4]	D[15:0]
		cycle 2:	{data[9:0],data[5:0]}	
YUV 422 8-bit	YUV 8-bit mode			D[15:8]
	YUV 422 8-bit alternative	{Y[7:0],UV[7:0]}[b]		D[15:0]
YUV 422 10-bit	YUV 10-bit mode			D[15:6]

a. data1, data2, and data3 can be L, S or VS depending on user mode

b. must keep PCLK as sensor SCLK

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HREF, VSYNC and PCLK are configured as video output port by default as in **figure 6-2**. The leading edge of VSYNC is triggered by an internal SOF signal and the interval between the internal SOF signal and VSYNC is controlled by v_sync_delay (0x4707~0x4709 in unit of PCLK periods). The VSYNC pulse width is set by registers 0x4702~0x4705 following the formula:

VSYNC width = [VSYNC width line × t_{Row}] + [VSYNC width pixel × t_{PCLK}]

where:

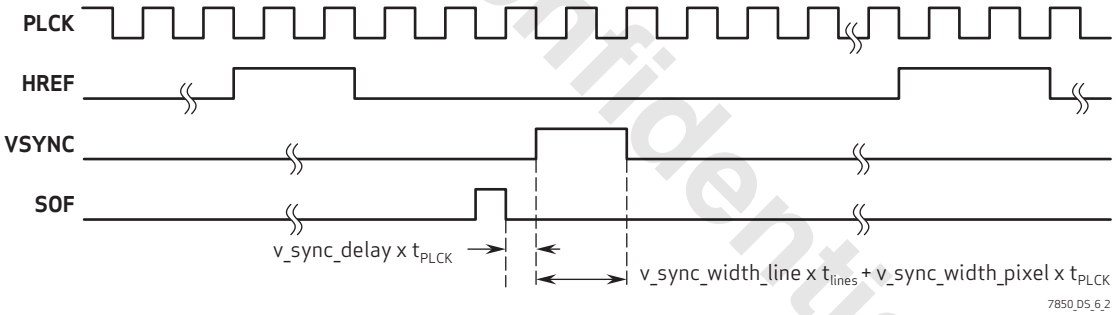
t_{Row} is row period,

t_{PCLK} is PCLK period.

VSYNC width line - 0x4702[1:0] high bits, 0x4703 low byte

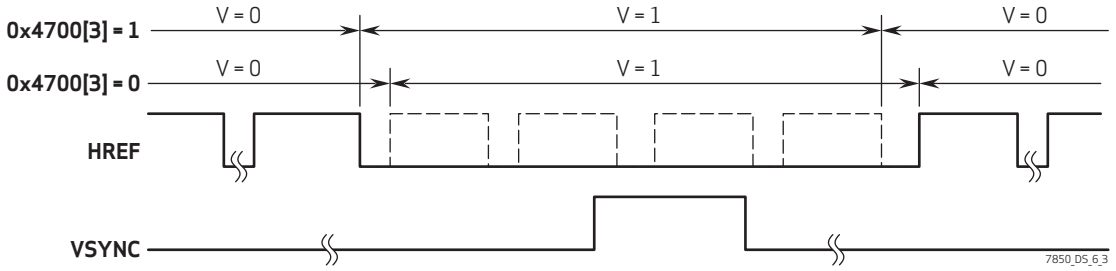
VSYNC width pixel - 0x4704[1:0] high bits, 0x4705 low byte

figure 6-2 mode 1 diagram



The OV7850 supports BT.656 embedded sync code, which is enabled by register 0x4700[1]. The field (F) bit in the sync code is set by register 0x4700[2] and is a fixed value because the output is always progressive. There is an option to for the vertical blanking (V) bit toggling between the blanking and active period as shown in **figure 6-3**.

figure 6-3 mode 2 diagram



The OV7850 supports walking one test pattern to test the connection between the sensor and the backend processor. The test pattern is enabled by register 0x470B[0]. By default, the image data bits are aligned with pins D[15:0].

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The driver strength of the DVP can be configured by 0x3011[7:6]. **table 6-4** shows the DVP setup/hold time at 56 MHz PCLK with 1x drive current.

figure 6-4 DVP setup/hold time diagram

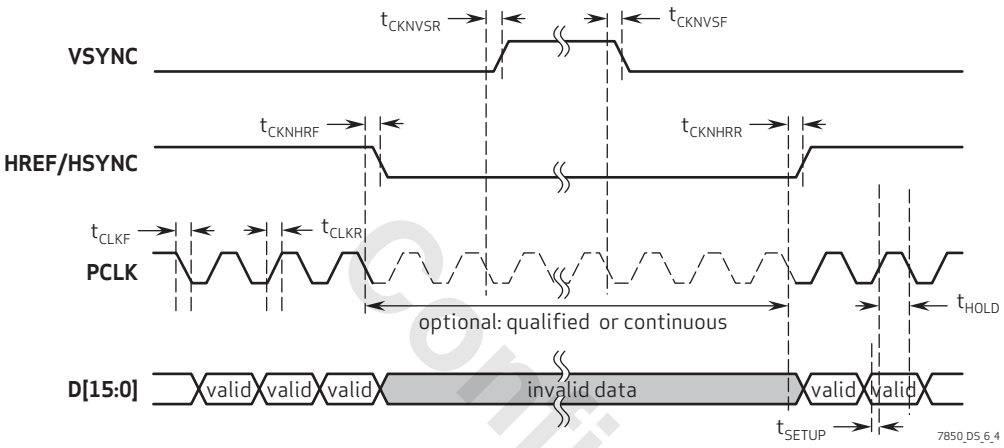

table 6-4 DVP setup/hold time[ab]

symbol	parameter	min	typ	max	unit
t_{CKNVSR}	PCLK falling edge to VSYNC rising edge delay	–	1.95	–	ns
t_{CKNVSF}	PCLK falling edge to VSYNC falling edge delay	–	1.76	–	ns
t_{CKNHRF}	PCLK falling edge to HREF falling edge delay	–	0.7	–	ns
t_{CKNHRR}	PCLK falling edge to HREF rising edge delay	–	0	–	ns
t_{CLKF}	PCLK fall time	0.29[c]	–	1.69[d]	ns
t_{CLKR}	PLCK rise time	0.29[c]	–	0.99[d]	ns
t_{SETUP}	data setup time	8.8	–	–	ns
t_{HOLD}	data hold time	7.6	–	–	ns

a. measured at 2.8V DOVDD and 96 MHz PCLK, with 2x drive strength

b. timing measurement shown at beginning of rising edge and/or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge and/or beginning of falling edge signifies 70%

c. 4x driving capability

d. 1x driving capability

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6.3 DVP timing

The DVP output is qualified by VSYNC and HREF and the timing is shown in **figure 6-5**.

figure 6-5 DVP timing diagram

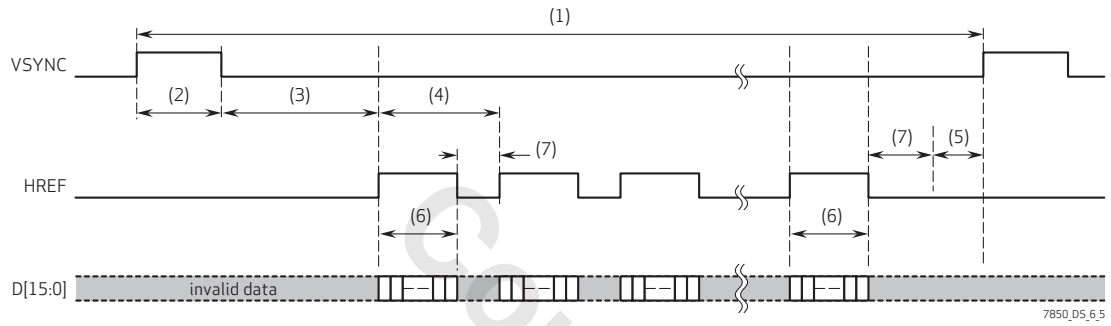

table 6-5 DVP timing specifications[a] (sheet 1 of 2)

resolution	parameter	format				
		HDR YUV 10-bit	combined RAW 18/20	RAW 2-channel	combined RAW 10/16	RAW 1-channel
744x520	(1) frame period	546 lines	546 lines	546 lines	546 lines	546 lines
	(2) VSYNC width	512 t_p	512 t_p	512 t_p	512 t_p	512 t_p
	(3) VSYNC to HREF	38322,5 t_p	34810,5 t_p	34772,5 t_p	17152 t_p	17132 t_p
	(4) line period	1676 t_p	1676 t_p	1676 t_p	838 t_p	838 t_p
	(5) HREF to VSYNC	4912 t_p	8424 t_p	8462 t_p	4209 t_p	4229 t_p
	(6) active pixel	1488 t_p	1488 t_p	1488 t_p	744 t_p	744 t_p
	(7) horizontal blanking	188 t_p	188 t_p	188 t_p	94 t_p	94 t_p
	(8) last horizontal blanking to VSYNC high	4740 t_p	8252 t_p	8290 t_p	4123 t_p	4143 t_p

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table 6-5 DVP timing specifications[a] (sheet 2 of 2)

resolution	parameter	format				
		HDR YUV 10-bit	combined RAW 18/20	RAW 2-channel	combined RAW 10/16	RAW 1-channel
640x480	(1) frame period	525 lines	525 lines	525 lines	525 lines	525 lines
	(2) VSYNC width	512 t_p	512 t_p	512 t_p	512 t_p	512 t_p
	(3) VSYNC to HREF	39250 t_p	35658,5 t_p	35618 t_p	17576 t_p	17558 t_p
	(4) line period	1716 t_p	1716 t_p	1716 t_p	858 t_p	858 t_p
	(5) HREF to VSYNC	37890,5 t_p	41482 t_p	41522,5 t_p	20738 t_p	20756 t_p
	(6) active pixel	1280 t_p	1280 t_p	1280 t_p	640 t_p	640 t_p
	(7) horizontal blanking	436 t_p	436 t_p	436 t_p	218 t_p	218 t_p
	(8) last horizontal blanking to VSYNC high	37454,5 t_p	41046 t_p	41086,5 t_p	20520 t_p	20538 t_p

a. These parameters change with different register settings.

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table 6-6 DVP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4700	MOD_SEL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Ccir656_blank_seq H-blank data toggle sequence 0: 80,10 1: 10,80 Bit[4:3]: Reserved Bit[2]: ccir656_f_value 0: 656's sync code fixed at field 0 1: 656's sync code fixed at field 1 Bit[1]: ccir656_mode_enable Bit[0]: Reserved
0x4701	LONG VSYNC MODE	0x00	RW	Bit[0]: Long VSYNC mode 0: Disable 1: Enable
0x4702	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[1:0]: VSYNC width by line number[9:8]
0x4703	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: VSYNC width by line number[7:0]

table 6-6 DVP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4704	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: VSYNC width by pixel number[15:8]
0x4705	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: VSYNC width by pixel number[7:0]
0x4706	VSYNC_MODE	0x00	RW	Bit[3:0]: Reserved
0x4707	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: VSYNC delay count[23:16]
0x4708	VSYNC_DELAY_M	0x00	RW	Bit[7:0]: VSYNC delay count[15:8]
0x4709	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: VSYNC delay count[7:0]
0x470A	POLARITY_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Bit reverse enable Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: Reserved Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity also PCLK gate low enable
0x470B	WALKING_1_TEST_PATTERN	0x00	RW	Bit[7]: Reserved Bit[6:4]: DVP data bit swap option Bit swap selection 1 (byp_select[5] = 0): 000: D[15:0] 001: D[0:15] 010: D[2:15], D[1:0] 011: D[4:15], D[3:0] 100: D[6:15], D[0:5] 101: D[8:15], D[0:7] 110: D[10:15], D[0:9] 111: D[12:15], D[0:11] Bit swap selection 2 (byp_select[5] = 1): 000: D[13:0], D[15:14] 001: D[11:0], D[15:12] 010: D[9:0], D[15:10] 011: D[7:0], D[15:8] 100: D[5:0], D[15:6] 101: D[3:0], D[15:4] 110: D[1:0], D[15:2] 111: 16'h0 Bit[3]: test_mode Bit[2]: test_bit10 Bit[1]: test_bit8 Bit[0]: test_enable

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table 6-6 DVP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x470C	BYP_SELECT	0x00	RW	Bit[5]: Choose DVP data bit swap selection in register 0x470B[6:4] 0: Bit swap selection 1 1: Bit swap selection 2 Bit[4]: href_sel Bit[3:0]: bypass_sel
0x470D	BYP_CTRL2	0x00	RW	Bit[5]: bypass_pclk Bit[4]: bypass_href Bit[3]: bypass_vsync Bit[2:0]: Bypass data[15:13]
0x470E	BYP_CTRL1	0x00	RW	Bit[7.0]: Bypass data[12:5]
0x470F	BYP_CTRL0	0x00	RW	Bit[7:3]: Bypass data[4:0] Bit[2]: bypass_gpio1 (sck pin) Bit[1]: bypass_gpio2 (sd_o pin) Bit[0]: bypass_gpio3 (sd_i pin)
0x4710	RSVD	–	–	Reserved

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6.3.1 long VSYNC DVP timing

The OV7850 supports long VSYNC mode where DVP output is qualified by VSYNC and HREF shown in **figure 6-6**. The long VSYNC timing is shown in **table 6-7**. To enable long VSYNC mode, set register 0x4701[0] to 1 and adjust the timing accordingly.

figure 6-6 long VSYNC DVP timing diagram

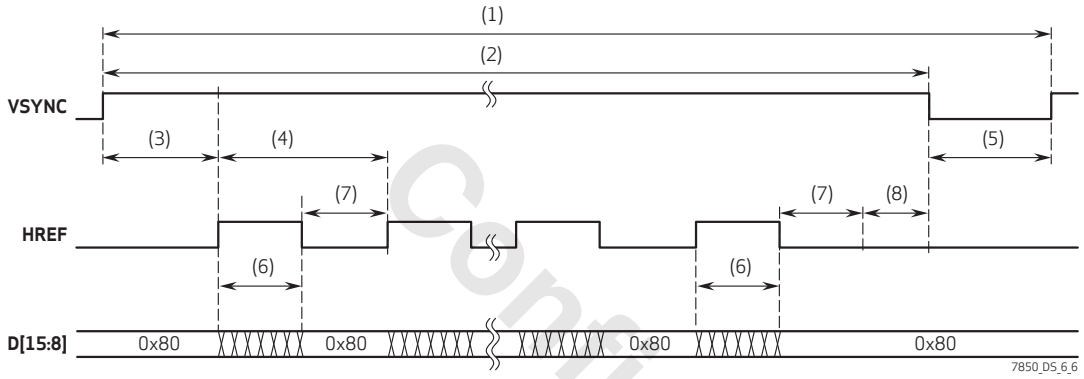

table 6-7 long VSYNC DVP timing specifications[a]

resolution	parameter	format		
		YUV 60 fps	YUV 30 fps	YUV 15 fps
640x480	(1) frame period	525 lines	525 lines	525 lines
	(2) VSYNC width	488 lines	488 lines	488 lines
	(3) VSYNC to HREF	7 lines	7 lines	7 lines
	(4) line period	1716 t_p	1716 t_p	1716 t_p
	(5) VSYNC low	37 lines	562 lines	1612 lines
	(6) active pixel	1280 t_p	1280 t_p	1280 t_p
	(7) horizontal blanking	436 t_p	436 t_p	436 t_p
	(8) last horizontal blanking to VSYNC low	1 line	1 line	1 line

a. t_p is PCLK period

VSYNC pulse width (high period = #lines + #pixels):

registers 0x4702~0x4703: #lines

registers 0x4704~0x4705: #pixels

VSYNC delay count (in #PCLK), delays VSYNC rising edge:

registers 0x4707~0x4709: #delay count

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6.4 TV mode

The OV7850 supports NTSC encoding. The analog output is driven by an on-chip current mode digital-to-analog (DAC) and the output current is converted to voltage by external termination resistors. If SCCB interface is not used, SIOC (SCCB clock) and SIOD (SCCB data) pins must be pulled up (10 Kohm) to DOVDD, either separately, or tied together and pulled up. An external resistor is also used to program the range of the DAC. The DAC output is CVBS differential signaling, which can be used to send to an analog NTSC capable display over long distances. It is enabled by default.

figure 6-7 NTSC timing diagram

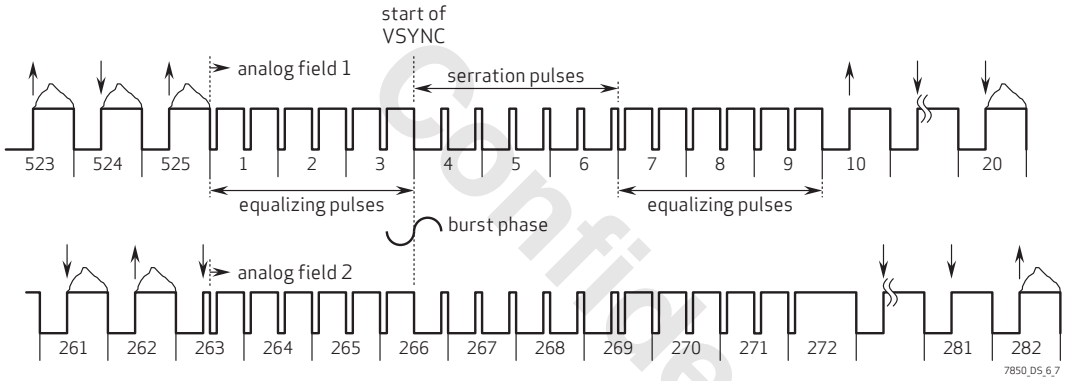

figure 6-8 NTSC composite video signal

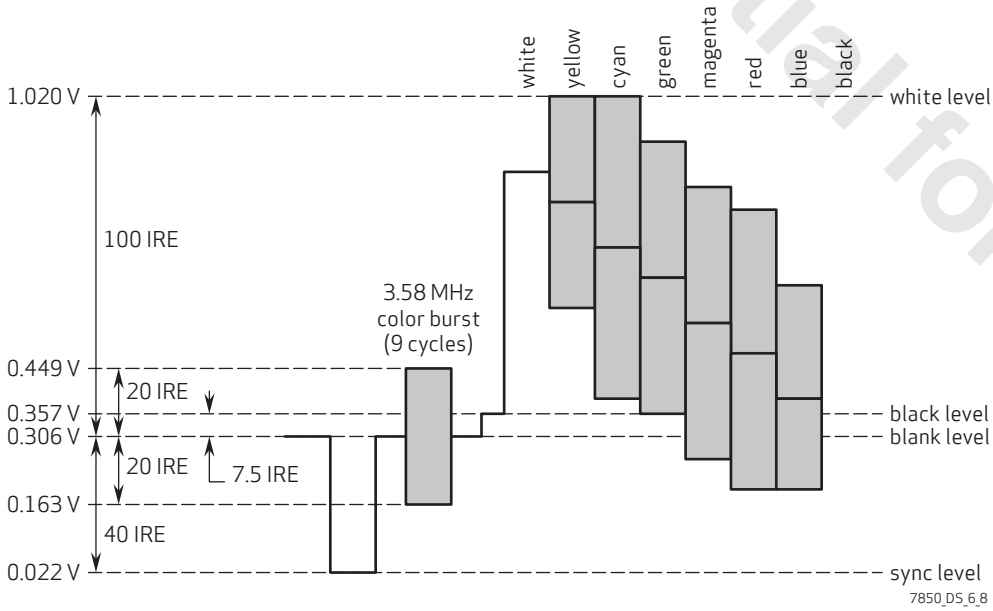

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table 6-8 TV encoder control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x4800	CVBS_CTRL_H	0x22	RW	Bit[7]: Test pattern Bit[6]: Progressive mode Bit[5]: Field option Bit[4]: Low pass filter enable Bit[3]: Reserved Bit[2]: Fixed phase Bit[1]: XSYNC option Bit[0]: PAL mode
0x4801	CVBS_CTRL_L	0x00	RW	Bit[7]: Oversample option, double sample DAC data Bit[6]: 27MHz system clock option Bit[5]: Reserved Bit[4]: YCbCr correction enable Bit[3]: NTSC 433 mode Bit[2]: Fixed DAC data enable Bit[1]: VSYNC option to reset TV timing Bit[0]: Reserved
0x4802	FIX_DATA_H	0x00	RW	Bit[1:0]: Fixed data output[9:8] When fixdata_en =1 (0x4801[2]), tvenc will output fixed data
0x4803	FIX_DATA_L	0x00	RW	Bit[7:0]: Fixed data output[7:0] When fixdata_en =1 (0x4801[2]), tvenc will output fixed data
0x4804	SCALING	0x00	RW	Bit[7:3]: Not used Bit[2]: FIFO read timing option, should be fixed in one project Bit[1:0]: Xscale option
0x4810	XSXOFFSET_H	0x00	RW	Bit[4:0]: X offset[12:8] Point on sensor timing domain to start TV timing counter
0x4811	XSXOFFSET_L	0x01	RW	Bit[7:0]: X offset[7:0] Point on sensor timing domain to start TV timing counter
0x4812	XSYOFFSET_H	0x02	RW	Bit[1:0]: Y offset[9:8] Point on sensor timing domain to start TV timing counter
0x4813	XSYOFFSET_L	0x0D	RW	Bit[7:0]: Y offset[7:0] Point on sensor timing domain to start TV timing counter
0x4814	WIDTH_H	0x06	RW	Bit[4:0]: TV output active image width[12:8]
0x4815	WIDTH_L	0x18	RW	Bit[7:0]: TV output active image width[7:0]
0x4816	HEIGHT_H	0x01	RW	Bit[1:0]: TV output active image height[9:8]

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table 6-8 TV encoder control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x4817	HEIGHT_L	0xE8	RW	Bit[7:0]: TV output active image height[7:0]
0x4820	VSTART1_H	0x00	RW	Bit[1:0]: Active image start line in TV timing field 1 (interlaced mode)[9:8]
0x4821	VSTART1_L	0x13	RW	Bit[7:0]: Active image start line in TV timing field 1 (interlaced mode)[7:0]
0x4822	VSTOP1_H	0x01	RW	Bit[1:0]: Active image end line in TV timing field 1 (interlaced mode)[9:8]
0x4823	VSTOP1_L	0x07	RW	Bit[7:0]: Active image end line in TV timing field 1 (interlaced mode)[7:0]
0x4824	VSTART2_H	0x01	RW	Bit[1:0]: Active image start line in TV timing field 2 (interlaced mode)[9:8]
0x4825	VSTART2_L	0x1A	RW	Bit[7:0]: Active image start line in TV timing field 2 (interlaced mode)[7:0]
0x4826	VSTOP2_H	0x02	RW	Bit[1:0]: Active image end line in TV timing field 2 (interlaced mode)[9:8]
0x4827	VSTOP2_L	0x0E	RW	Bit[7:0]: Active image end line in TV timing field 2 (interlaced mode)[7:0]
0x4828	VSTART3_H	0x00	RW	Bit[1:0]: Active image start line in TV timing (progressive mode)[9:8]
0x4829	VSTART3_L	0x18	RW	Bit[7:0]: Active image start line in TV timing (progressive mode)[7:0]
0x482A	VSTOP3_H	0x01	RW	Bit[1:0]: Active image end line in TV timing (progressive mode)[9:8]
0x482B	VSTOP3_L	0xF8	RW	Bit[7:0]: Active image end line in TV timing (progressive mode)[7:0]
0x482C	SCSHIFT_3	0x25	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482D	SCSHIFT_2	0x55	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482E	SCSHIFT_1	0x55	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482F	SCSHIFT_0	0x63	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x4830	WHITELEVEL_H	0x03	RW	Bit[1:0]: Maximum luminance signal level on TV (for 10-bit encoder)[9:8]
0x4831	WHITELEVEL_L	0xFF	RW	Bit[7:0]: Maximum luminance signal level on TV (for 10-bit encoder)[7:0]

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table 6-8 TV encoder control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x4832	NORMLEVEL_H	0x01	RW	Bit[1:0]: Minimum luminance signal level on TV (for 10-bit encoder)[9:8]
0x4833	NORMLEVEL_L	0x1A	RW	Bit[7:0]: Minimum luminance signal level on TV (for 10-bit encoder)[7:0]
0x4834	BLANKLEVEL_H	0x00	RW	Bit[1:0]: Blanking level on TV[9:8]
0x4835	BLANKLEVEL_L	0xF0	RW	Bit[7:0]: Blanking level on TV[7:0]
0x4836	SYNCSTEPS	0x02	RW	Bit[7:0]: Step number when blanking level switching to sync level
0x4837	BURSTSTEPS	0x02	RW	Bit[7:0]: Step number for burst level changing
0x4838	SYNCLEVEL_H	0x00	RW	Bit[1:0]: Sync level on TV[9:8]
0x4839	SYNCLEVEL_L	0x10	RW	Bit[7:0]: Sync level on TV[7:0]
0x483A	BURSTLEVEL_H	0x00	RW	Bit[1:0]: Amplitude of burst on TV[9:8]
0x483B	BURSTLEVEL_L	0x73	RW	Bit[7:0]: Amplitude of burst on TV[7:0]
0x483C	SYNCDELTA_H	0x00	RW	Bit[1:0]: Syncdelta[9:8] (blank level - sync level) / sync_steps
0x483D	SYNCDELTA_L	0x70	RW	Bit[7:0]: Syncdelta[7:0] (blank level - sync level) / sync_steps
0x483E	BURSTDELTA_H	0x00	RW	Bit[1:0]: Burstdelta[9:8] Burst level / burst step
0x483F	BURSTDELTA_L	0x38	RW	Bit[7:0]: Burstdelta[7:0] Burst level / burst step
0x4840	HCSYNCON_H	0x00	RW	Bit[4:0]: TV line counter value of horizontal sync start point[12:8]
0x4841	HCSYNCON_L	0x1D	RW	Bit[7:0]: TV line counter value of horizontal sync start point[7:0]
0x4842	HCSYNCOFF_H	0x00	RW	Bit[4:0]: TV line counter value of horizontal sync end point[12:8]
0x4843	HCSYNCOFF_L	0x91	RW	Bit[7:0]: TV line counter value of horizontal sync end point[7:0]
0x4844	HCBURSTON_H	0x00	RW	Bit[4:0]: TV line counter value of burst start point[12:8]
0x4845	HCBURSTON_L	0x9F	RW	Bit[7:0]: TV line counter value of burst start point[7:0]

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table 6-8 TV encoder control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x4846	HCBURSTOFF_H	0x00	RW	Bit[4:0]: TV line counter value of burst end point[12:8]
0x4847	HCBURSTOFF_L	0xDD	RW	Bit[7:0]: TV line counter value of burst end point[7:0]
0x4848	HCACTIVEON_H	0x00	RW	Bit[4:0]: TV line counter value of active pixel start point[12:8]
0x4849	HCACTIVEON_L	0xFA	RW	Bit[7:0]: TV line counter value of active pixel start point[7:0]
0x484A	HCACTIVEOFF_H	0x06	RW	Bit[4:0]: TV line counter value of active pixel end point[12:8]
0x484B	HCACTIVEOFF_L	0x0A	RW	Bit[7:0]: TV line counter value of active pixel end point[7:0]
0x484C	HCVALIDON_H	0x00	RW	Bit[4:0]: TV line counter value of valid start point[12:8]
0x484D	HCVALIDON_L	0xFA	RW	Bit[7:0]: TV line counter value of valid start point[7:0]
0x484E	HCVALIDOFF_H	0x06	RW	Bit[4:0]: TV line counter value of valid end point[12:8]
0x484F	HCVALIDOFF_L	0x0A	RW	Bit[7:0]: TV line counter value of valid end point[7:0]
0x4850	MINLEVEL_H	0x00	RW	Bit[1:0]: Minimum level of DAC input data[9:8]
0x4851	MINLEVEL_L	0x01	RW	Bit[7:0]: Minimum level of DAC input data[7:0]
0x4852	MAXLEVEL_H	0x03	RW	Bit[1:0]: Maximum level of DAC input data[9:8]
0x4853	MAXLEVEL_L	0xFF	RW	Bit[7:0]: Maximum level of DAC input data[7:0]
0x4854~ 0x4857	RSVD	–	–	Reserved
0x4858	CHROMASAT_H	0x01	RW	Bit[0]: Chroma signal saturation level[8]
0x4859	CHROMASAT_L	0xFF	RW	Bit[7:0]: Chroma signal saturation level[7:0]
0x485A	RSVD	–	–	Reserved
0x485B	FETCH_OFFS	0x03	RW	Bit[7:0]: Horizontal FIFO data fetch signal offset
0x4860~ 0x487F	RSVD	–	–	Reserved

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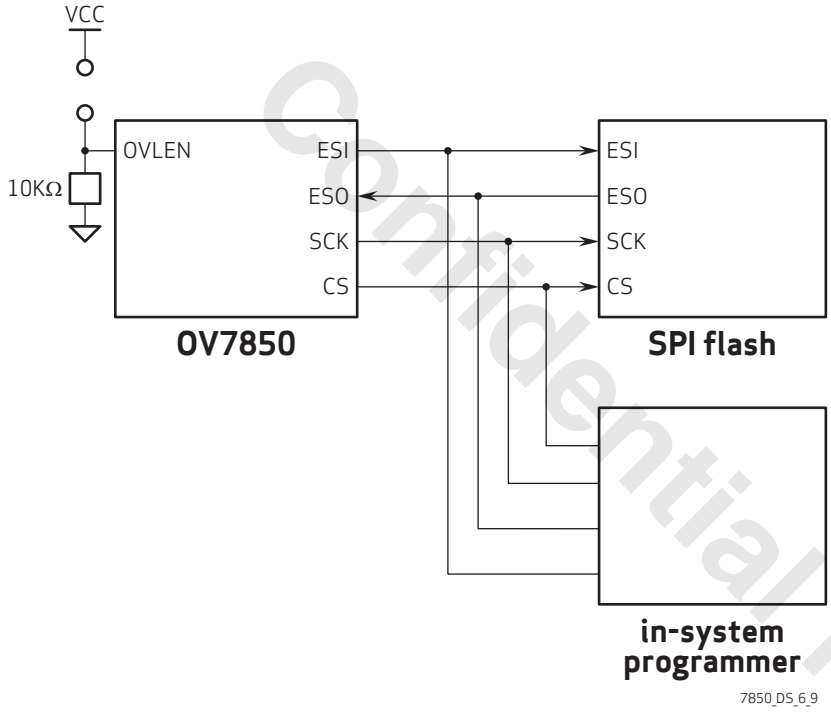
6.5 overlay (OSD)

On-screen display (OSD) bitmaps may be overlaid onto the video stream. Two simultaneous channels are available, each capable of overlaying one bitmap per frame. Bitmap data is stored in a SPI flash device. The overlay function is enabled by register 0x620D[0].

6.5.1 hardware connection

figure 6-9 in-system programer



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On the hardware level, the connection from the OV7850 to serial flash is through a standard SPI interface. The OV7850 supports in-system programming of SPI flash. Pull down OVLEN pin and all four pins on the SPI port will become inputs; thus, enabling an external downloader to program the flash. They change to tri-state when powered down.

6.5.2 internal overlay structure

The overlay image is read in from SPI flash on a line-by-line, on-demand basis. Once inside, it is decompressed and mixed with pixel data. Up to two overlay images can be mixed in succession to produce the final output.

figure 6-10 overlay channels

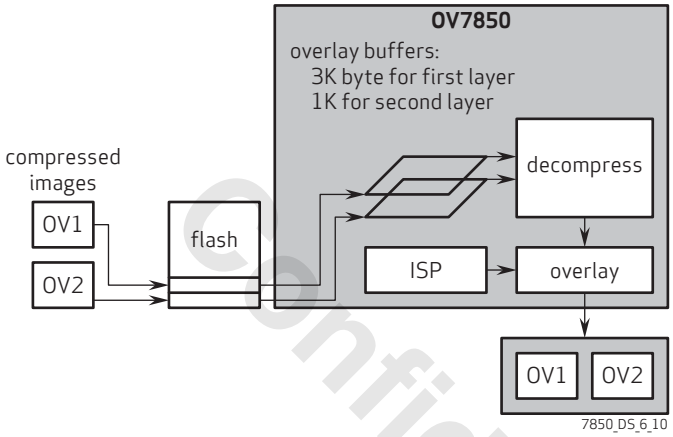
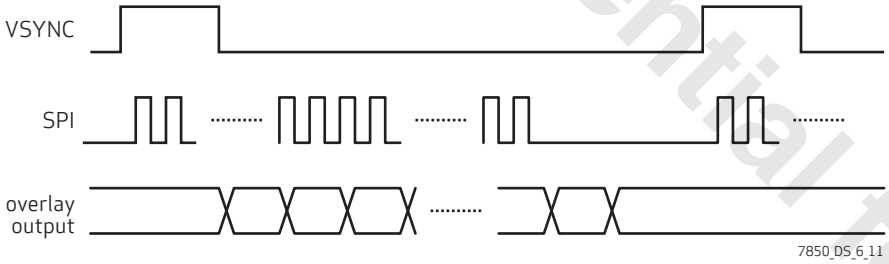


figure 6-11 relative timing



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6.5.3 flash memory structure

The memory structure supports bitmap format in B&W. It also supports the storage of register settings. For detailed overlay setting and memory structure, please contact your local OmniVision FAE.

table 6-9 OSD control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x6200	R_ADDR_BYTE	0x02	RW	Bit[1:0]: Byte address space of SPI EEPROM 00: 1 byte 01: 2 bytes 10: 3 bytes 11: 4 bytes
0x6201	R_SCK_POL	0x00	RW	Bit[0]: ESCK polarity rev
0x6202	R_SPEED	0x04	RW	Bit[4:0]: EEPROM read speed 0x0: ESCK speed = pclk* 0x1: ESCK speed = pclk/2 0x2: ESCK speed = pclk/4 Others: PCLK freq = 2×sclk freq
0x6203	EOF_CLR	0x00	RW	Bit[0]: End of frame clear signal 0: Use SOF as overlay image load start for each frame 1: Use previous EOF as overlay image load start for each frame
0x6204	GRP_HLD	0x00	RW	Bit[0]: Group hold register 0: Index or resolution information load is allowed for each layer 1: Cannot load until grp_hold changes to 0
0x6205	R_FRAME_COM	0x00	RW	Bit[0]: Frame compress mode 0: Compress one line mode frame compress. Need to read in overlay image information at beginning of a line. 1: Compress whole frame mode. Read in all overlay image information at beginning of a frame. There is no SPI interface in use during a frame.
0x6206	R_DLY	0x02	RW	Bit[4:0]: spi_ctrl request delay Adjust delay timing between two SPI control requests
0x6207~ 0x6208	RSVD	–	–	Reserved

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table 6-9 OSD control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x6209	R_FAST_RD	0x01	RW	Bit[0]: Fast read command select signal to make read command faster When enabled, corresponding fast read command should be 8'h0B (0x620F).
0x620A	R_ROUND_BACK	0x01	RW	Bit[0]: SPI read-in data and valid timing option
0x620B	R_GATE_EN	0x01	RW	Bit[0]: Internal SCK gate option
0x620D	R_OSD_CTRL	0x01	RW	Bit[1:0]: OSD control 0: Enable OSD function 1: Bypass OSD function
0x620E	RSVD	–	–	Reserved
0x620F	R_FAST_RD_CMD	0x0B	RW	Bit[7:0]: Fast read instruction Default is 8'h0B, synchronize with 0x6209
0x6210	R_RD_CMD	0x03	RW	Bit[7:0]: Normal read instruction Synchronize with 0x6209
0x6211	R_INDEX0_T_L	0x01	RW	Bit[7:0]: Overlay image 0 index[7:0]
0x6212	R_INDEX1_T_L	0x02	RW	Bit[7:0]: Overlay image 1 index[7:0]
0x6213~ 0x6214	RSVD	–	–	Reserved
0x6215	R_INDEX0_T_H	0x00	RW	Bit[1:0]: Overlay image 0 index[9:8]
0x6216	R_INDEX1_T_H	0x00	RW	Bit[1:0]: Overlay image 1 index[9:8]
0x6217~ 0x6218	RSVD	–	–	Reserved
0x6219	R_OV_RESO0_T	0x00	RW	Bit[1:0]: Image resolution for layer1 0: Overlay image disabled 1: Overlay image resolution 1x1
0x621A	R_OV_RESO1_T	0x00	RW	Bit[1:0]: Resolution for layer1
0x621B~ 0x621C	RSVD	–	–	Reserved
0x621D	R_X_START0_T_L	0x00	RW	Bit[7:0]: X start address for layer 0[7:0]
0x621E	R_Y_START0_T_L	0x00	RW	Bit[7:0]: Y start address for layer 0[7:0]
0x621F	R_X_START0_T_H	0x00	RW	Bit[3:0]: X start address for layer 0[11:8]
0x6220	R_Y_START0_T_H	0x00	RW	Bit[3:0]: Y start address for layer 0[11:8]
0x6221	R_X_START1_T_L	0x00	RW	Bit[7:0]: X start address for layer 1[7:0]

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table 6-9 OSD control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x6222	R_Y_START1_T_L	0x00	RW	Bit[7:0]: Y start address for layer 1[7:0]
0x6223	R_X_START1_T_H	0x00	RW	Bit[3:0]: X start address for layer 1[11:8]
0x6224	R_Y_START1_T_H	0x00	RW	Bit[3:0]: Y start address for layer 1[11:8]
0x6225~ 0x622C	RSVD	–	–	Reserved
0x622D	SCCB_WDATA	0x00	RW	Bit[7:0]: SCCB write data
0x622E	LAY0_SEL	0x00	RW	Bit[1:0]: Layer0 select 00: Select image0 stored in EEPROM as layer0 image 01: Select image1 stored in EEPROM as layer0 image 10: Select image2 stored in EEPROM as layer0 image (this number has to be a valid image number in EEPROM or load image will fail)
0x622F	LAY1_SEL	0x01	RW	Bit[1:0]: Layer1 select 00: Select image0 stored in EEPROM as layer1 image 01: Select image1 stored in EEPROM as layer1 image 10: Select image2 stored in EEPROM as layer1 image (this number has to be a valid image number in EEPROM or load image will fail)
0x6230~ 0x6231	RSVD	–	–	Reserved
0x6232	R_LD_INDEX	0x00	RW	Bit[7:0]: Loading index 00: Select setting 0 stored in EEPROM to load 01: Select setting 1 stored in EEPROM to load 10: Select setting 2 stored in EEPROM to load (this number has to be a valid setting file number in EEPROM or load setting function will fail)
0x6233	R_AUTOMOVY_EN0	0x00	RW	Bit[0]: Y auto move function enable for layer0
0x6234	R_AUTOMOVY_EN1	0x00	RW	Bit[0]: Y auto move function enable for layer1
0x6235~ 0x6236	RSVD	–	–	Reserved

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table 6-9 OSD control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x6237	R_AUTOMOVX_EN0	0x00	RW	Bit[0]: X auto move function enable for layer0
0x6238	R_AUTOMOVX_EN1	0x00	RW	Bit[0]: X auto move function enable for layer1
0x6239~ 0x623A	RSVD	–	–	Reserved
0x623B	R_AUTOMOVY_ WRAP_EN0	0x00	RW	Bit[0]: Auto move function Y wrap enable for layer0
0x623C	R_AUTOMOVY_ WRAP_EN1	0x00	RW	Bit[0]: Auto move function Y wrap enable for layer1
0x623D~ 0x623E	RSVD	–	–	Reserved
0x623F	R_AUTOMOVX_ WRAP_EN0	0x00	RW	Bit[0]: Auto move function X wrap enable for layer0
0x6240	R_AUTOMOVX_ WRAP_EN1	0x00	RW	Bit[0]: Auto move function X wrap enable for layer1
0x6241~ 0x6242	RSVD	–	–	Reserved
0x6243	R_AUTOMV_STEP_ SEL	0x00	RW	Bit[0]: Auto move step select 0: Step enabled 1: Step only enabled at frames with auto change step pre-defined
0x6244	RSVD	–	–	Reserved
0x6245	R_SPI_SELN	0x00	RW	Bit[0]: SPI load select
0x6246	R_LD_PAD_DIS	0x00	RW	Bit[0]: Load pad disable
0x6247	R_LD_TRIGGER	0x01	RW	Bit[1:0]: Load trigger control 0: Power on load disable 1: Manual load setting function trigger
0x6248	RSVD	–	–	Reserved
0x6249	R_RETRY	0x02	RW	Bit[1:0]: Loading settings retry times
0x624A	R_SEQ_NU	0xFF	RW	Bit[7:0]: OSD_SEQ sequencer byte number
0x624B	R_TOGCNT_OR_ RBLANKLINENU	0x20	RW	Bit[7:0]: Toggle counter or blanking lines number
0x624C	R_READ_ONCE0	0x00	RW	Bit[0]: FIFO write enable and FIFO read enable select signal for layer0
0x624D	R_READ_ONCE1	0x00	RW	Bit[0]: FIFO write enable and FIFO read enable select signal for layer1

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table 6-9 OSD control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x624E~ 0x624F	RSVD	–	–	Reserved
0x6250	R_RETRY_PON	0x01	RW	Bit[0]: Retry only when power on
0x6251	RSVD	–	–	Reserved
0x6252	R_LD_BLANK	0x01	RW	Bit[0]: Loading blank 0: Do not load setting until blanking 1: Load setting at any time
0x6253	R_AUTOCHG_ WRAP_EN0	0x00	RW	Bit[0]: Auto change wrap enable for layer0
0x6254	R_AUTOCHG_ WRAP_EN1	0x00	RW	Bit[0]: Auto change wrap enable for layer1
0x6255~ 0x6256	RSVD	–	–	Reserved
0x6257	R_AUTOCHG_EN0	0x00	RW	Bit[0]: Auto change enable for layer0
0x6258	R_AUTOCHG_EN1	0x00	RW	Bit[0]: Auto change enable for layer1
0x6259~ 0x625A	RSVD	–	–	Reserved
0x625B	R_AUTOCHG_ STIDX0_L	0x00	RW	Bit[7:0]: Auto change start index for layer0[7:0]
0x625C	R_AUTOCHG_ EDIDX0_L	0x00	RW	Bit[7:0]: Auto change end index for layer0[7:0]
0x625D	R_AUTOCHG_ STIDX1_L	0x00	RW	Bit[7:0]: Auto change start index for layer1[7:0]
0x625E	R_AUTOCHG_ EDIDX1_L	0x00	RW	Bit[7:0]: Auto change end index for layer1[7:0]
0x625F~ 0x6262	RSVD	–	–	Reserved
0x6263	R_AUTOCHG_ STIDX0_H	0x00	RW	Bit[1:0]: Auto change start index for layer0[9:8]
0x6264	R_AUTOCHG_ EDIDX0_H	0x00	RW	Bit[1:0]: Auto change end index for layer0[9:8]
0x6265	R_AUTOCHG_ STIDX1_H	0x00	RW	Bit[1:0]: Auto change start index for layer1[9:8]
0x6266	R_AUTOCHG_ EDIDX1_H	0x00	RW	Bit[1:0]: Auto change end index for layer1[9:8]

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table 6-9 OSD control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x6267~ 0x626A	RSVD	–	–	Reserved
0x626B	R_AUTOCHG_STEP _L	0x00	RW	Bit[7:0]: Auto change step[7:0]
0x626C	R_AUTOCHG_STEP _H	0x00	RW	Bit[7:0]: Auto change step[15:8]
0x626D	R_AUTOMOVY_ STEP0	0x00	RW	Bit[3:0]: Auto move Y step for layer0
0x626E	R_AUTOMOVX_ STEP0	0x00	RW	Bit[3:0]: Auto move X step for layer0
0x626F	R_AUTOMOVY_ STEP1	0x00	RW	Bit[3:0]: Auto move Y step for layer1
0x6270	R_AUTOMOVX_ STEP1	0x00	RW	Bit[3:0]: Auto move X step for layer1
0x6271~ 0x6274	RSVD	–	–	Reserved
0x6275	OSD_ERR_ST_H	–	R	Bit[7:0]: OSD error state[15:8]
0x6276	OSD_ERR_ST_L	–	R	Bit[7:0]: OSD error state[7:0]
0x627F	R_YUV_Y_VAL	0x03	RW	Bit[1:0]: Overlay image Y low 2 bits added value
0x6280	R_LD_WB_ADRHI_ H	0x00	RW	Bit[7:0]: Wishbone address bus[15:8] for load setting function
0x6281	R_LD_WB_ADRHI_L	0x06	RW	Bit[7:0]: Wishbone address bus[7:0] for load setting function
0x6282	R_LD_DONE_O	–	R	Bit[0]: Flag to indicate load setting process is done
0x6283	R_OVEN_PAD_O	–	R	Bit[0]: Read only signal of oven pad value

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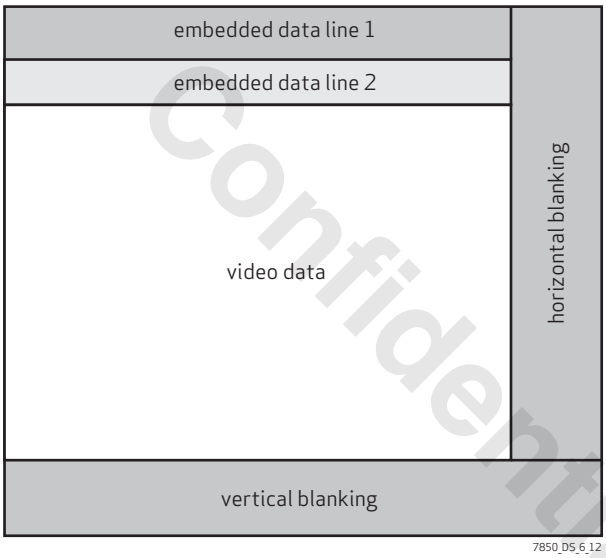
6.6 embedded row

Additional information about the set up and configuration of the sensor can be embedded in the video stream. The embedded data contains the values of a programmable list of registers to describe the current state of the sensor (e.g., the frame counter, exposure time and gain etc.). The embedded data function is enabled when register 0x381D[2]=1.

The embedded data is always the two rows before the valid video data.

figure 6-12 embedded line video stream



The register address to include in the embedded data is defined in the embedded line table. In the OV7850, there are four data ranges to input the embedded data. The start address and end address for these four ranges are given in registers 0x320A~0x3219.

6.6.1 configuration of embedded data

There are 13 user configurable groups and 17 fixed values output in the embedded line.

The first three groups have programmable register range, defined by a start and end address (see **table 6-10**). The OV7850 will output continuous values in the embedded line selected from the range start and end registers.

Group1 outputs 24 WB gain registers by default (0x5080-0x5097). When embedded data format is DADA XXXX, their locations are at 02, 06, 10…94.

Group 2 outputs 16 AWB statistics registers by default (0x58D0-0x58DF). When embedded data format is DADA XXXX, their locations are at 98, 102, 106…158

Group 3 outputs 30 BLC statistics registers by default (0x4014-0x4031). When embedded data format is DADA XXXX, their locations are at 162, 166, 170…278

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table 6-10 register range configuration

parameter	group 1 max 24 register		group 2 max 16 registers		group 3 max 30 registers	
relative location in embedded line	02, 06, 10…94		98, 102, 106…158		162, 166, 170…278	
start address MSB	0x320A	0x50[a]	0x320E	0x58[a]	0x3212	0x40[a]
start address LSB	0x320B	0x80[a]	0x320F	0xD0[a]	0x3213	0x14[a]
end address MSB	0x320C	0x50[a]	0x3210	0x58[a]	0x3214	0x40[a]
end address LSB	0x320D	0x97[a]	0x3211	0xDF[a]	0x3215	0x31[a]

a. sensor register range to output in embedded line

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The last 10 user programmable groups can output up to 10 register values in the embedded line (see **table 6-11**). The registers values to output are programmed through registers 0x1F00 to 0x1F2F. Before accessing 0x1Fxx registers, a different page must be selected by setting register 0xFFF9 to 0x01. After access of 0x1Fxx registers is complete, register 0xFFF9 must be set back to 0x06. Every three registers define one group with start address (MSB and LSB) and register number. Only the relative data location is fixed and the total maximum programmable length is 10.

table 6-11 register range for embedded line

group	address	sensor range to output in embedded line
4	0x1F00	address MSB
	0x0F01	address LSB
	0x1F02	register number
5	0x1F03	address MSB
	0x1F04	address LSB
	0x1F05	register number
...	...	...
13	0x1F2D	address MSB
	0x1F2E	address LSB
	0x1F2F	register number

The 10 location offset is: 120, 124, 136, 140, 152, 156, 168, 172, 184, 188. The relative location is: base + offset. Base means the first three group sum. By default, it is 278.

Example:

```
One group with 10 register address

0x1f00 35; address MSB

0x1f00 00; address LSB

0x1f02 0a; read 10 consecutive register from 0x3500


Two groups with 5 register address

0x1f00 35; address MSB

0x1f00 00; address LSB

0x1f02 05; read 5 consecutive register from 0x3500

0x1f00 30; address MSB

0x1f00 00; address LSB

0x1f02 05; read 5 consecutive register from 0x3000
```

There are also 17 fixed register values summarized in **table 6-12**.

table 6-12 fixed register values

sensor register output in embedded line		offset
ABC frame indicator	0x381B	04
frame counter	{0x3886, 0x3887}	08, 12
long exposure	{0x3500, 0x3501}	20, 24
long gain	0x3505	28
short exposure	{0x3502, 0x3503}	36, 40
short gain	0x3506	44
very short exposure	0x3504	56
very short gain	0x3507	60
AEC/AGC statistics	{0x5AE2, 0x5AE3}	72, 76
long/short/very short black level	{0x500D, 0x500F, 0x5011}	88, 92, 104
temperature	0x6719	108

The relative location is: base + offset. Base means the first three group sum. By default, it is 278.

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By default the embedded line will be as summarized in **table 6-13** when enabled:

table 6-13 embedded line register range

parameter	address	number of bytes	address in embedded line
frame counter	0x3886, 0x3887	2	286, 290
ABC frame indicator	0x381B	1	282
temperature	0x6719	1	386
AEC/AGC statistics	0x5AE2, 0x5AE3	2	350, 354
long, short, VS exposure	0x3500~0x3504	5	298, 302, 314, 318, 334
long, short, VS gain	0x3505~0x3507	3	306, 322, 338
AWB statistics	0x58D0~0x58DF	16	98, 102, …158
AWB gain & offset	0x5080~0x5097	24	02, 06…,94
BLC statistics	0x4014~0x4031	30	162, 166, …278
BLC target	0x500D, 0x500F, 0x5011	3	366, 370, 382
user define	0x1F00~0x1F2F	10	398, …466

6.6.2 embedded data row timing

The embedded data is output when HREF is asserted and before each register value that is output. In 8-bit output mode every register value is tagged with 0xDA as shown in **figure 6-13** to avoid conflict with CCIR656 header and embedded line data format:

- YUV: DADA XXXX DADA XXXX
- RAW: DA XX DA XX

For 10-bit output mode, two bit zero will be added to the tag. Tag = {0xDA,2'b00}, value= {0xDA,2'b00}

It is important to note that the embedded data tag and register value change per pixel, so in YUV mode, with 2xPCLK frequency, the embedded tag and data will be stable for two PCLK periods. In the timing diagram, the Val0 is the first register value in the embedded data, Val1 is the second, etc. The output of embedded data will always stop after two lines and also when the definition of the register fields to output as embedded data exceeds the number of available cycles.

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figure 6-13 embedded data row timing diagram

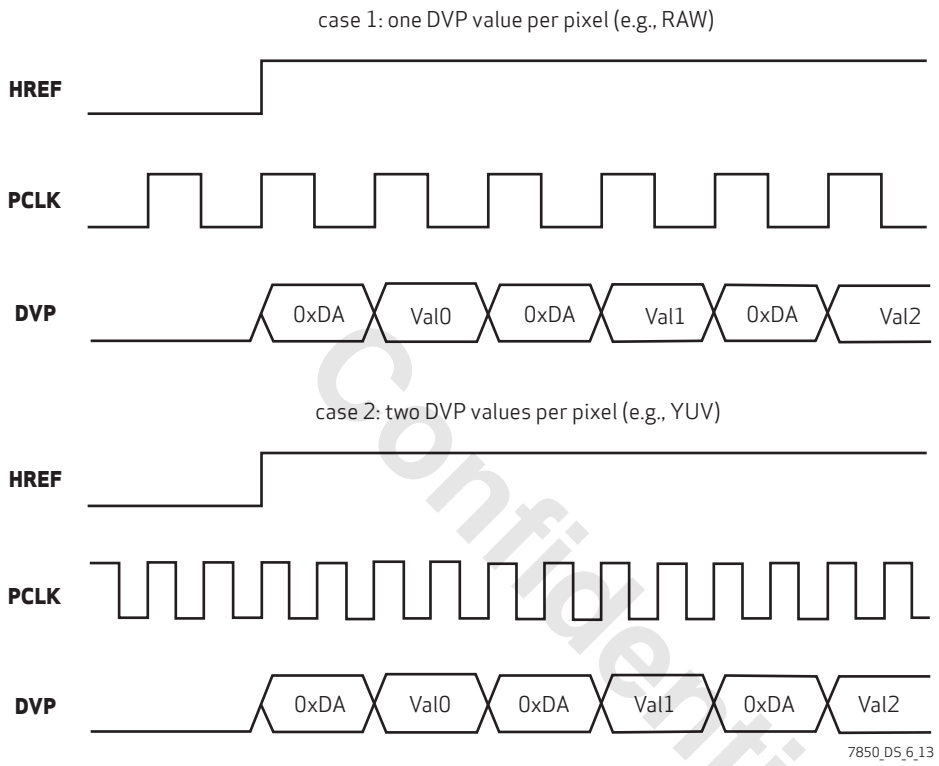

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table 6-14 embedded line control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x320A	EMB_START_ADDR0_ H	0x0F	RW	Bit[7:0]: High address for first embedded data range 0
0x320B	EMB_START_ADDR0_L	0x30	RW	Bit[7:0]: Low address for first embedded data range 0
0x320C	EMB_END_ADDR0_H	0x0F	RW	Bit[7:0]: High address for last embedded data range 0
0x320D	EMB_END_ADDR0_L	0xBF	RW	Bit[7:0]: Low address for last embedded data range 0
0x320E	EMB_START_ADDR1_H	0x40	RW	Bit[7:0]: High address for first embedded data range 1 Change to FF if not used

table 6-14 embedded line control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320F	EMB_START_ADDR1_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 1 Change to FF if not used
0x3210	EMB_END_ADDR1_H	0x40	RW	Bit[7:0]: High address for last embedded data range 1
0x3211	EMB_END_ADDR1_L	0x3B	RW	Bit[7:0]: Low address for last embedded data range 1
0x3212	EMB_START_ADDR2_H	0x38	RW	Bit[7:0]: High address for first embedded data range 2 Change to FF if not used
0x3213	EMB_START_ADDR2_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 2 Change to FF if not used
0x3214	EMB_END_ADDR2_H	0x38	RW	Bit[7:0]: High address for last embedded data range 2
0x3215	EMB_END_ADDR2_L	0x8D	RW	Bit[7:0]: Low address for last embedded data range 2
0x381D	READ_CTRL	0x04	RW	Bit[7:3]: Not used Bit[2]: show_embedded_rows Bit[1]: show_test_rows Bit[0]: show_black_rows

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6.7 group hold

The OV7850 supports group hold mode in which the register values are recorded in an internal buffer instead of writing to the register directly. The SCCB enters group hold mode after register 0x3204[7] is set. Then, all subsequent registers (except 0x3204) are recorded to the group hold registers until register 0x3204[7] is cleared. When enabling group launch, the associated sensor registers are updated with the register values in the specified group before the start of next frame as set in register 0x3204.

The OV7850 supports up to four groups. The buffer size (number of entries) for each group is set by registers 0x3200~0x3203. The total sum for the four groups is limited to 768 entries (i.e., 256 registers values). For each register to program, there are three entries:

- 16 bit register address:
  - 1 byte MSB
  - 1 byte LSB
- 8 bit register value

table 6-15 group hold buffer size

group	register	number of entries	number of registers
0	0x3200	255	255/3 = 85
1	0x3201	255	255/3 = 85
2	0x3202	129	129/3 = 43
3	0x3203	129	129/3 = 43

The group hold function can launch only once or switch between two or three groups. This function is controlled by register 0x3207[1:0].

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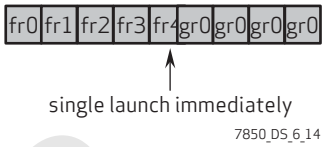
6.7.1 single start, set 0x3207[1:0] = 00

Program group settings into registers 0x3200~0x3203 and choose which group to launch in 0x3204[3:2]. Group settings will launch only once and a new write is required to launch additional group settings. The user can choose to launch:

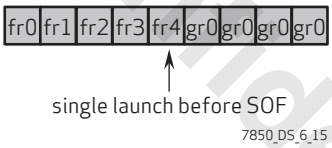
- immediately, which might result in broken frame.

figure 6-14 broken frame example



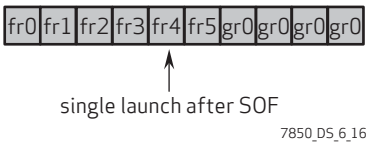
- before sensor core SOF, group register values will take effect following frame.

figure 6-15 launch before sensor core SOF example



- after sensor core SOF, group register values will take after following frame.

figure 6-16 launch after sensor core SOF example



6.7.2 auto mode, set 0x3207[1:0] = 01 (ABC mode)

This mode automatically switches between two or three (AB or ABC set by 0x5502) mode group settings using frame counts. The user programs group settings into registers 0x3200~0x3203, then chooses which two groups to switch between. The group switch will take effect after following frame.

figure 6-17 auto mode example

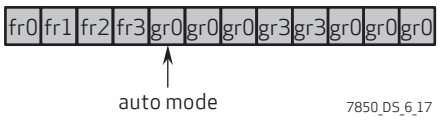


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table 6-16 group hold control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP_LENGTH0	0xFF	RW	Bit[7:0]: Number of registers for group 0, total sum of 4 groups is limited to 768
0x3201	GROUP_LENGTH1	0xFF	RW	Bit[7:0]: Number of registers for group 1
0x3202	GROUP_LENGTH2	0x81	RW	Bit[7:0]: Number of registers for group 2
0x3203	GROUP_LENGTH3	0x81	RW	Bit[7:0]: Number of registers for group 3
0x3204	GROUP_CTRL	0x13	RW	Bit[7]: Hold register writes Bit[6]: Launch immediately, when single_start is set Bit[5]: Launch before sensor core SOF, if single_start is set Bit[4]: Launch after sensor core SOF, if single_start is set Bit[3:2]: Main group select for hold and launch operation (also used as first group in auto mode) 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: Used as second group in auto mode
0x3205	FIRST_GRP_FRAMES	0x01	RW	Bit[7:0]: Frames for staying in group selected by first group selected
0x3206	SECOND_GRP_FRAMES	0x01	RW	Bit[7:0]: Frames for staying in group selected by second group selected
0x3207	OPERATION_CTRL	0x02	RW	Bit[1]: Auto mode Bit[0]: Single start
0x3208	ACTIVE_GROUP_NR	–	R	Bit[1:0]: Indicates which group is active
0x3209	FRAME_CNT_ACTIVE	–	R	Bit[7:0]: Number of frames with current group (valid only in auto mode)
0x320A	EMB_START_ADDR0_H	0x0F	RW	Bit[7:0]: High address for first embedded data range 0
0x320B	EMB_START_ADDR0_L	0x30	RW	Bit[7:0]: Low address for first embedded data range 0
0x320C	EMB_END_ADDR0_H	0x0F	RW	Bit[7:0]: High address for last embedded data range 0
0x320D	EMB_END_ADDR0_L	0xBF	RW	Bit[7:0]: Low address for last embedded data range 0
0x320E	EMB_START_ADDR1_H	0x40	RW	Bit[7:0]: High address for first embedded data range 1 Change to FF if not used.

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table 6-16 group hold control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320F	EMB_START_ADDR1_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 1 Change to FF if not used.
0x3210	EMB_END_ADDR1_H	0x40	RW	Bit[7:0]: High address for last embedded data range 1
0x3211	EMB_END_ADDR1_L	0x3B	RW	Bit[7:0]: Low address for last embedded data range 1
0x3212	EMB_START_ADDR2_H	0x38	RW	Bit[7:0]: High address for first embedded data range 2 Change to FF if not used.
0x3213	EMB_START_ADDR2_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 2 Change to FF if not used.
0x3214	EMB_END_ADDR2_H	0x38	RW	Bit[7:0]: High address for last embedded data range 2
0x3215	EMB_END_ADDR2_L	0x8D	RW	Bit[7:0]: Low address for last embedded data range 2
0x3216	EMB_START_ADDR3_H	0xFF	RW	Bit[7:0]: High address for first embedded data range 3 Change to FF if not used.
0x3217	EMB_START_ADDR3_L	0xFF	RW	Bit[7:0]: Low address for first embedded data range 3 Change to FF if not used
0x3218	EMB_END_ADDR3_H	0x36	RW	Bit[7:0]: High address for last embedded data range 3
0x3219	EMB_END_ADDR3_L	0x1F	RW	Bit[7:0]: Low address for last embedded data range 3
0x3220	FORCE_BUS_DELAY	0x0C	RW	Bit[3:0]: In module embedded data, delay from start of early VSYNC until register is forced busy

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7 serial camera control bus (SCCB) interface

The SCCB interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for data transfer protocol and detailed usage of the serial control port.

7.1 SCCB timing

figure 7-1 SCCB interface timing

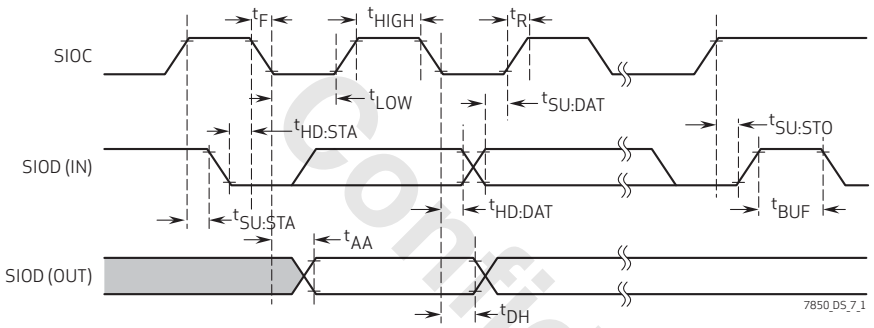

table 7-1 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SIOC}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SIOC low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz mode

b. timing measurement shown at beginning of rising edge or end of falling edge signifies 30%,
timing measurement shown in middle of rising/falling edge signifies 50%,
timing measurement shown at end of rising edge or beginning of falling edge signifies 70%

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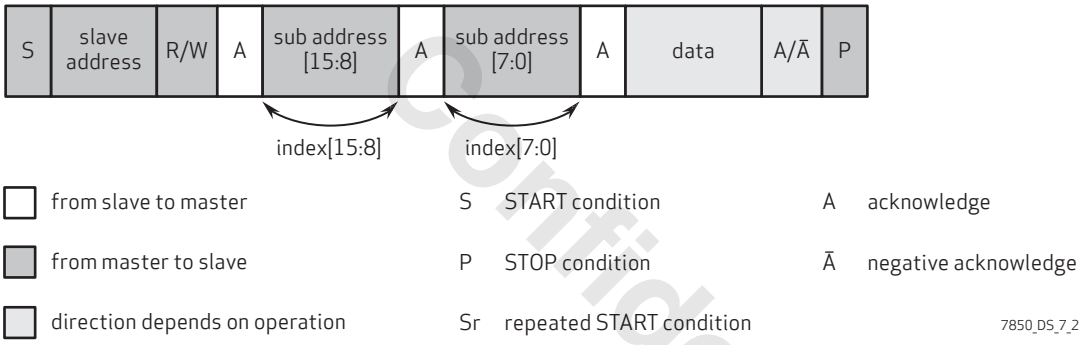
7.2 direct access mode

7.2.1 message format

The OV7850 supports the message format shown in **figure 7-2**. The repeated START (Sr) condition is shown in **figure 7-3** and **figure 7-5**.

figure 7-2 message type

message type: 16-bit sub-address, 8-bit data, and 7-bit slave address



7.2.2 read / write operation

The OV7850 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SIOD line as shown in **figure 7-3**. The master terminates the read operation by setting a negative acknowledge and stop condition.

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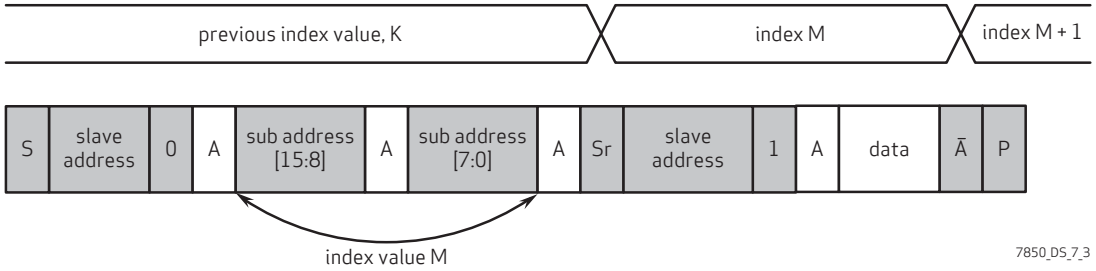
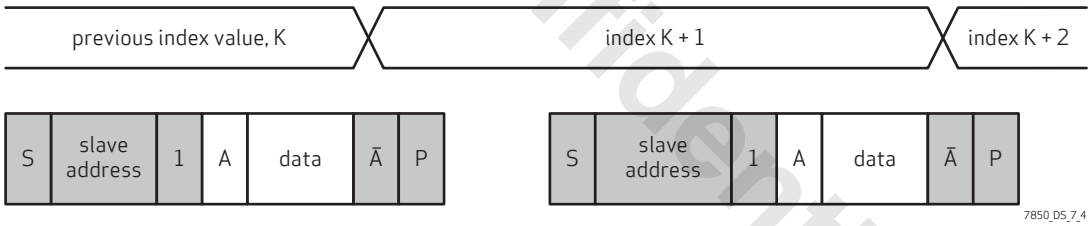
figure 7-3 SCCB single read from random location



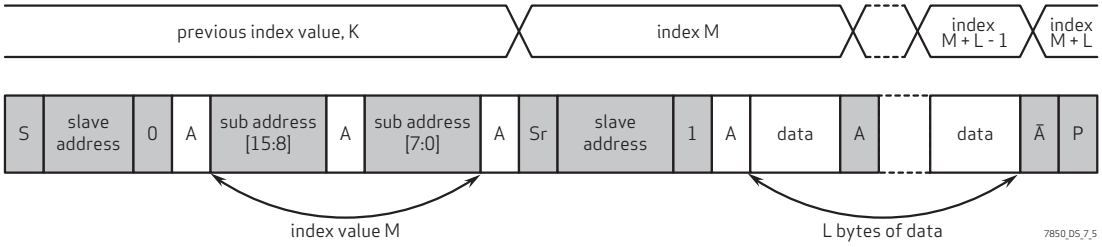
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SIOD line as shown in **figure 7-4**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 7-4 SCCB single read from current location



The sequential read from a random location is illustrated in **figure 7-5**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 7-5 SCCB sequential read from random location



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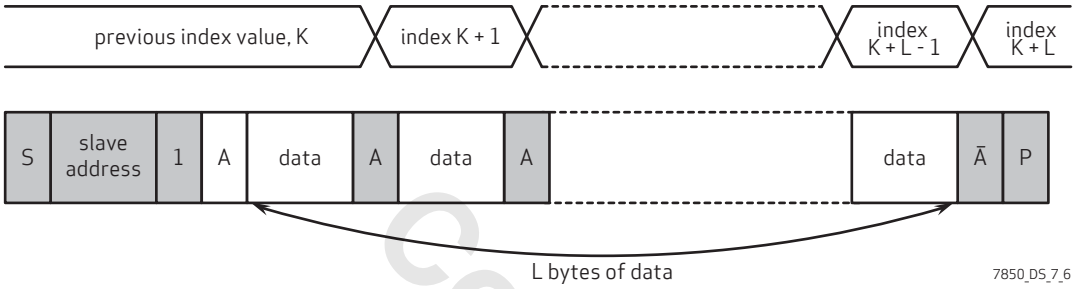
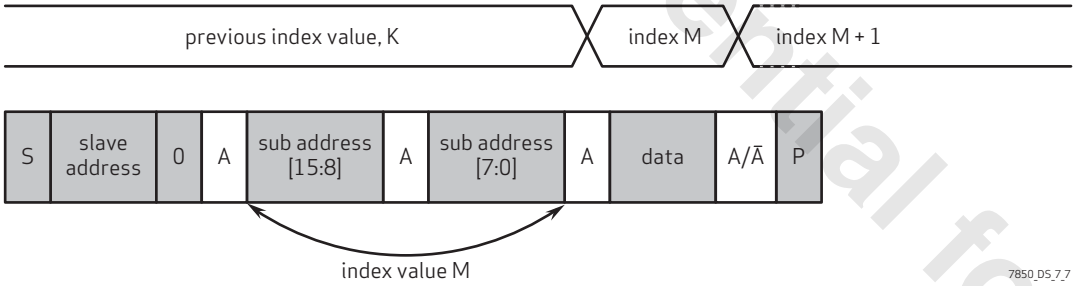
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation as shown in **figure 7-6**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 7-6 SCCB sequential read from current location



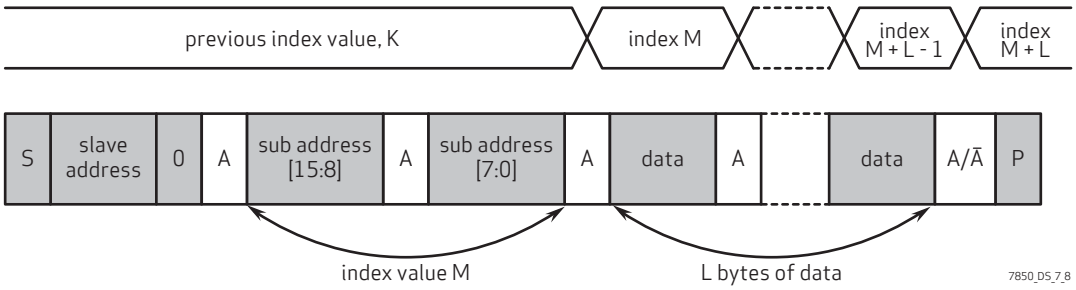
The write operation to a random location is illustrated in **figure 7-7**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 7-7 SCCB single write to random location



The sequential write is illustrated in **figure 7-8**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 7-8 SCCB sequential write to random location



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8 miscellaneous functions

8.1 OTP memory

The OV7850 integrates 32 bytes of OTP memory. The memory is used to store production information to trace each part and is also used to store the calibration data for internal functions (e.g., the temperature offset). The OTP is controlled through the SCCB interface and OTP control registers in**table 8-1**.

The OTP is organized as 2 banks. Each bank consists of 128 bits, which can be accessed by 16 registers. The first bank is used by OmniVision. The bank select is through register 0x3D84[5:0], where 0 means accessing bank (OTP memory location) 0, and 1 means accessing bank 1. The OTP register buffers which are used to program/read the OTP values are 0x3D00~0x3D0F.

In auto mode (0x3D84[6]=0) when register 0x3D80 is set to 0x01, the OTP enters program mode and the data in OTP register buffers are sequentially burned into the OTP. When register 0x3D81 is set to 0x01, the OTP enters read mode, and data in OTP is read out and loaded into OTP register buffers. Since the OTP memory can only be programmed once, the user should be very careful accessing the OTP.

The OTP values in the register buffers can also be programmed in manual mode (0x3D84[6]=1) by specifying register buffer range manually. The register buffer start address is set in register 0x3D85 and end address in register 0x38D6, the range can be anything between 0x00 and 0x0F, with 0x3D84 specifying which bank to program.

The automatic read and write access is described in **section 8.1.1** and **section 8.1.2**.

8.1.1 procedure to read OTP content

1. Clear software buffer which is used to receive OTP content
1. Start video streaming
1. Clear OTP register buffers 0x3D00~0x3D0F to 0x00.
2. Set register 0x3D84 to 0x00 or 0x01 for bank 0 or bank 1.
3. Set register 0x3D81 to 0x01 to initiate OTP read (read command).
4. Wait 25ms.
5. Read OTP values from register buffers 0x3D00~0x3D0F.

8.1.2 procedure to program OTP content

1. Follow **section 8.1.1,** procedure to read OTP content, to make sure the OTP is blank.
2. Write the OTP values into register buffers 0x3D00~0x3D0F.
3. Set register 0x3D84 to 0x00 or 0x01 for bank 0 or bank 1.
4. Set register 0x3D80 0x01 to initiate OTP programming (program command).
5. Wait 60ms. Any register access during this period is prohibited.
6. Follow the **section 8.1.1,** procedure to read OTP content, to read back the OTP content.
7. Compare the OTP content read back to the intended OTP content.

The OTP memory is programmed using analog power. The AVDD voltage for OTP programming must be 2.5V ± 10%. The power supply should be able to provide extra 50mA for OTP programming.

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figure 8-1 OTP diagram

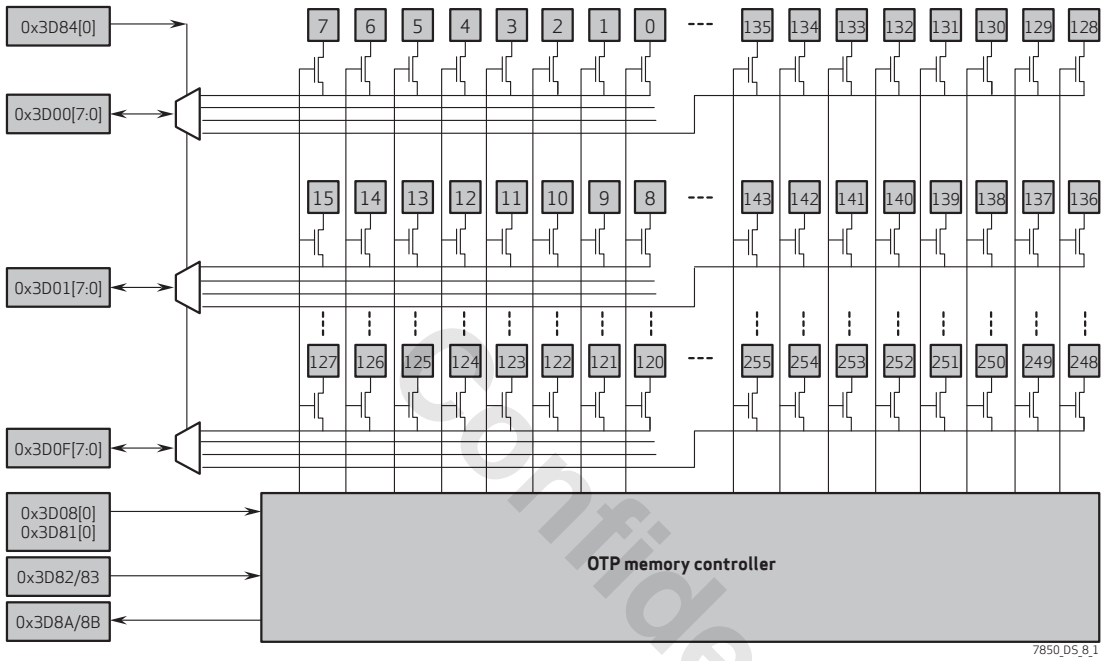

table 8-1 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D00	OTP_BYTE0	0x00	RW	OTP Write/read Buffer 0
0x3D01	OTP_BYTE1	0x00	RW	OTP Write/read Buffer 1
0x3D02	OTP_BYTE2	0x00	RW	OTP Write/read Buffer 2
0x3D03	OTP_BYTE3	0x00	RW	OTP Write/read Buffer 3
0x3D04	OTP_BYTE4	0x00	RW	OTP Write/read Buffer 4
0x3D05	OTP_BYTE5	0x00	RW	OTP Write/read Buffer 5
0x3D06	OTP_BYTE6	0x00	RW	OTP Write/read Buffer 6
0x3D07	OTP_BYTE7	0x00	RW	OTP Write/read Buffer 7
0x3D08	OTP_BYTE8	0x00	RW	OTP Write/read Buffer 8
0x3D09	OTP_BYTE9	0x00	RW	OTP Write/read Buffer 9
0x3D0A	OTP_BYTE10	0x00	RW	OTP Write/read Buffer 10

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table 8-1 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D0B	OTP_BYTE11	0x00	RW	OTP Write/read Buffer 11
0x3D0C	OTP_BYTE12	0x00	RW	OTP Write/read Buffer 12
0x3D0D	OTP_BYTE13	0x00	RW	OTP Write/read Buffer 13
0x3D0E	OTP_BYTE14	0x00	RW	OTP Write/read Buffer 14
0x3D0F	OTP_BYTE15	0x00	RW	OTP Write/read Buffer 15
0x3D80	R_PGM_CTR	0x00	RW	Bit[0]: otp_pgm Program start signal Write 1 this register to start programing
0x3D81	R_LOAD_CTR	0x00	RW	Bit[0]: otp_rd Read start signal Write 1 this register to start load data
0x3D82	R_PGM_PULSE	0x40	RW	Bit[7:0]: Program pulse Control load strobe pulse by Tsclk
0x3D83	R_LOAD_PULSE	0x03	RW	Bit[3:0]: Load pulse Control load strobe pulse by Tsclk
0x3D84	R_MODE_CTRL	0x40	RW	Bit[7]: program_dis Value = 1 to disable programing Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: Memory select Used to choose exact one 000000: Select memory 1 000001: Select memory 2 Others: Not used
0x3D85	R_START_ADDRESS	0x00	RW	Bit[3:0]: Start address for manual mode
0x3D86	R_END_ADDRESS	0x0F	RW	Bit[3:0]: End address for manual mode
0x3D87	R_PS2CS	0x03	RW	Bit[3:0]: PS to CSB time control, by sclk
0x3D88	LD_WR_GAP	0x08	RW	Bit[7:0]: Load write register gap
0x3D89	LOAD_CTRL	0x00	RW	Bit[7:0]: OTP load setting enable
0x3D8A	R_OTP_PROG_O	–	R	Bit[0]: otp_prog_o 1: Programming
0x3D8B	R_OTP_LOAD_O	–	R	Bit[0]: otp_load_o 1: Loading

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8.2 temperature sensor

The OV7850 has an embedded temperature sensor to measure junction temperature. This temperature sensor requires a 1-3 MHz clock divided from XVCLK. The temperature monitor is disabled by register 0x3852[4].

The temperature can be read back from register 0x6719. When the value is below 0xC0, it is the temperature in Celsius. When the value is greater than 0xC0, the temperature is (0x6719) - 0x100 in Celsius.

The slope and offset of the temperature sensor is calibrated in an OmniVision production test and the calibration data is stored in the OTP. After calibration, the accuracy of the temperature reading is ±5 degree Celsius over the operating temperature range. When the temperature is out of the operating temperature range, the reading from the temperature sensor is not reliable and is for reference only.

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9 operating specifications

9.1 absolute maximum ratings

table 9-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-50°C to +125°C
supply voltage (analog)	V_{DD-A}	4.5V
supply voltage (digital circuit)	V_{DD-D}	2V
supply voltage (digital I/O + AVDD)	V_{DD-IO}	4.5V
analog I/O (VMON, VMONL, VH, ATEST, VRES, VCON, VCOP)		-0.3V to V_{DD-A}
all digital I/O		-0.3V to V_{DD-IO}
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

9.2 functional temperature

table 9-2 functional temperature

parameter	range
operating temperature[a]	-30°C to +85°C junction temperature
stable image temperature	0°C to +50°C junction temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes

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9.3 DC characteristics

table 9-3 DC characteristics (-30°C < T_J < +85°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-D}	supply voltage (digital circuit)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}[a]			45	60	mA
I_{DD-D}	active (operating) current[b]		130	250	mA
I_{DD-IO}			15	50	mA
$I_{DDS-PWDN-A}$[c]			10	20	µA
$I_{DDS-PWDN-D}$	standby current[d]		150	300	µA
$I_{DDS-PWDN-IO}$			10	30	µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[e]	SIOC and SIOD	-0.5	0	.45	V
V_{IH}[e]	SIOC and SIOD	1.05	1.5	1.95	V

a. analog current including SVDD

b. OmniVision recommends adding an external heat sink in order to reduce chip temperature

c. standby current without input clock

d. standby current based on room temperature

e. based on DOVDD = 1.8V.

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9.4 AC characteristics

table 9-4 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth	3		4	MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			1	ms
	settling time for register setting			32	ms

table 9-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5	ns

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9.5 DAC electrical characteristics

table 9-6 video DAC electrical characteristics single-ended mode

symbol	parameter	min	typ	max	unit
EXTCLK = 24MHz, DVDD = 1.5V, OVDD = 3.3V, DAC_REF (register 0x3850[3:0]) = 0x8, T_J = -40° to 125°C					
resolution			10		bits
DNL			0.2	0.35	bits
INL			0.7	2	bits
output local load	output pad (VCOP)		75		Ω
	unused output (VCON)		75		Ω
output voltage	single-ended mode, code 000h	0.37	0.27	1.75[a]	V
	single-ended mode, code 3FFh	1.25	1.28	1.32	V
output current	single-ended mode, code 000h	4.88	4.97	23.28[a]	nA
	single-ended mode, code 3FFh	16.68	17.10	17.62	mA
supply current		18.4	18.8	19.4	mA
DAC_REF	DAC reference	–	1.19	–	V
R_DAC_REF	DAC reference	–	1375[b]	–	Ω

a. at T_J = 125°

b. DAC reference current is programmed by DAC_REF/(R_DAC_REF+R_wire)), where R_wire is an internal routing resistance approximated to 31 Ω

table 9-7 video DAC electrical characteristics differential mode (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
EXTCLK = 24MHz, DVDD = 1.5V, OVDD = 3.3V, DAC_REF (register 0x3850[3:0]) = 0x8, T_J = -40° to 125°C					
DNL			0.2	0.35	bits
INL			0.7	2	bits
output local load	differential mode per pad (VCOP and VCON)		75		Ω

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table 9-7 video DAC electrical characteristics differential mode (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
output voltage	differential mode, code 000h, VOP	0.37	0.37	1.75[a]	µV
	differential mode, code 000h, VON	1.25	1.28	1.32	V
	differential mode, code 3FFh, VOP	1.25	1.28	1.32	V
	differential mode, code 3FFh, VON	0.37	0.37	1.75[a]	µV
output current	differential mode, code 000h, VOP	4.88	4.97	23.28[a]	nA
	differential mode, code 000h, VON	16.68	17.10	17.62	mA
	differential mode, code 3FFh, VOP	16.68	17.10	17.62	mA
	differential mode, code 3FFh, VON	4.88	4.97	23.28[a]	nA
differential output, mid level		0.626	0.641	0.661	V
supply current		18.4	18.8	19.4	mA
DAC_REF	DAC reference	–	1.19	–	V
R_DAC_REF	DAC reference	–	1375[b]	–	Ω

a. at T_J = 125°

b. DAC reference current is programmed by DAC_REF/(R_DAC_REF+R_wire)), where R_wire is an internal routing resistance approximated to 31 Ω

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10 mechanical specifications

10.1 physical specifications

figure 10-1 package specifications

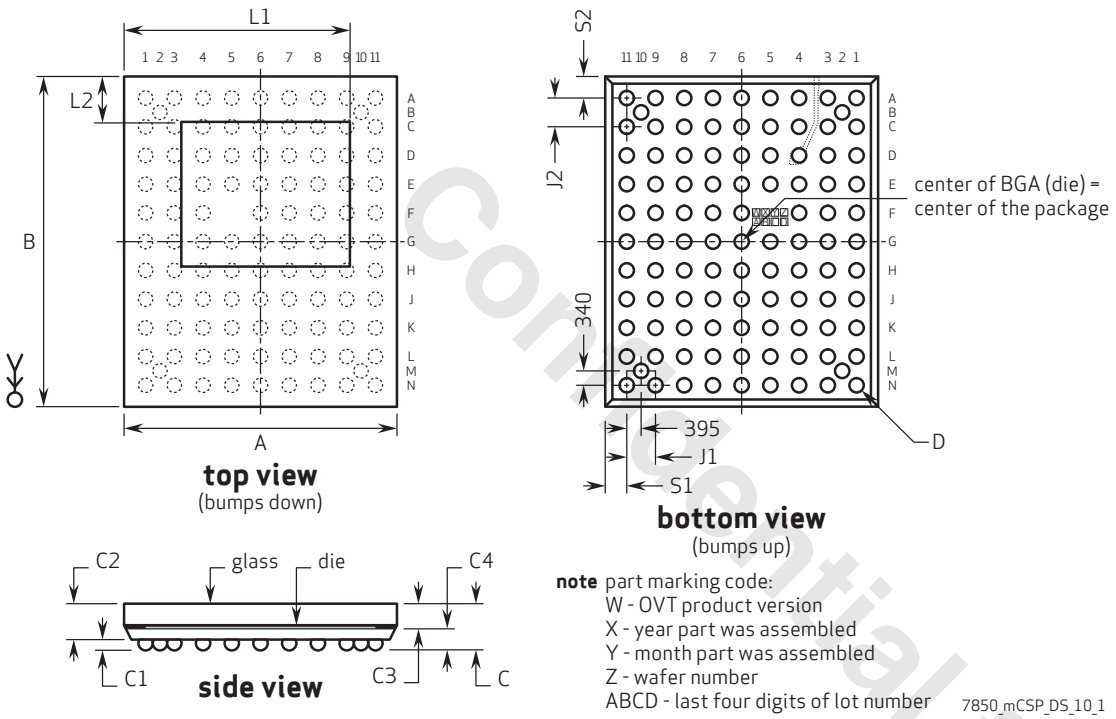

table 10-1 package dimensions (sheet 1 of 2)

parameter	symbol	min	typ	max	unit
package body dimension x	A	7285	7310	7335	µm
package body dimension y	B	7785	7810	7835	µm
package height	C	915	975	1035	µm
pixel to package edge dimension A	L1	6074	6109	6144	µm
pixel to package edge dimension B	L2	1058	1093	1128	µm
ball height	C1	315	345	375	µm
package body thickness	C2	585	630	675	µm
thickness of glass surface to wafer	C3	425	445	465	µm

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table 10-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
image plane height	C4	475	530	585	µm
ball diameter	D	385	415	445	µm
total pin count	N		102		
pin count x-axis	N1		11		
pin count y-axis	N2		13		
pins pitch x-axis	J1		790		µm
pins pitch y-axis	J2		680		µm
edge-to-pin center distance along x	S1	465	495	525	µm
edge-to-pin center distance along y	S2	475	505	535	µm
air gap between die and glass		40	45	50	µm
tilt between die and glass				0.2	degree
die rotation				0.1	degree

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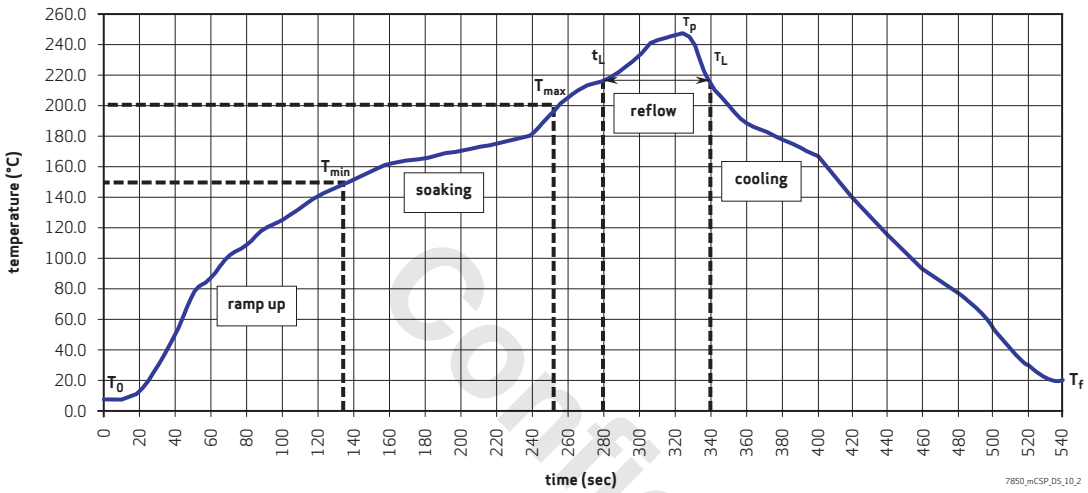
10.2 IR reflow specifications

figure 10-2 IR reflow ramp rate requirements



note
The OV7850 uses a lead free package.

note
OmniVision recommends mCSP packages use underfill as part of camera assembly process.

table 10-2 reflow conditions[ab]

zone	description	exposure
ramp up A (T_0 to T_{min})	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	90 ~ 150 seconds
ramp up B (t_L to T_P)	heating from 217°C to 245°C	temperature slope ≤ 3°C per second
peak temperature	maximum temperature in SMT	245°C +0/-5°C (duration max 30 sec)
reflow (t_L to T_L)	temperature higher than 217°C	30 ~ 120 seconds
ramp down A (T_P to T_L)	cooling from 245°C to 217°C	temperature slope ≤ 3°C per second
ramp down B (T_L to T_f)	cooling from 217°C to room temperature	temperature slope ≤ 2°C per second
T_0 to T_P	room temperature to peak temperature	≤ 8 minutes

a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas PPM<500 as recommendation

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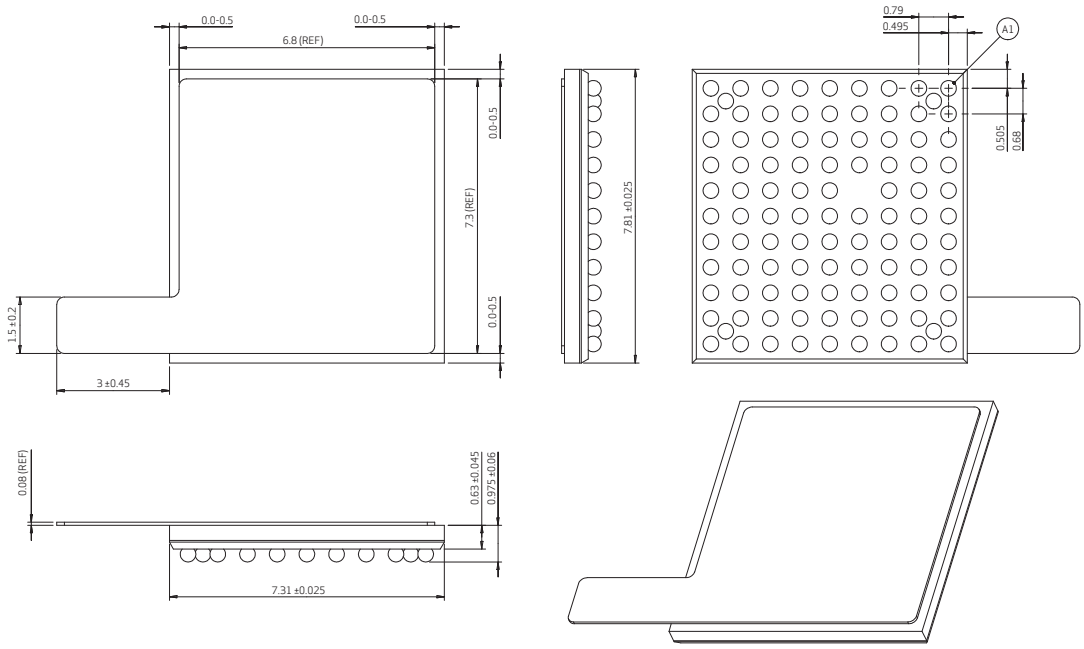
10.3 protective film specifications

figure 10-3 protective film specifications



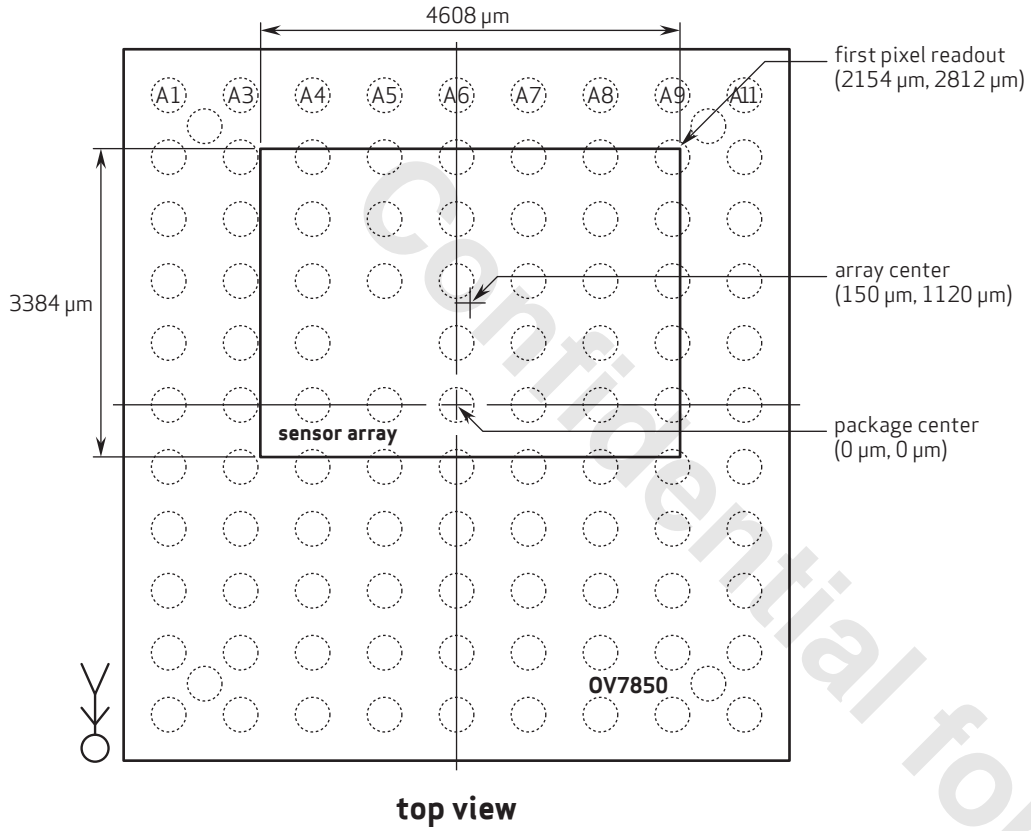
note all dimensions are in millimeters unless otherwise specified.

7850_mCSP_DS_10_3

11 optical specifications

11.1 sensor array center

figure 11-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 oriented down on the PCB.

7850_mCSP_DS_11_1

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11.2 lens chief ray angle (CRA)

figure 11-2 chief ray angle (CRA)

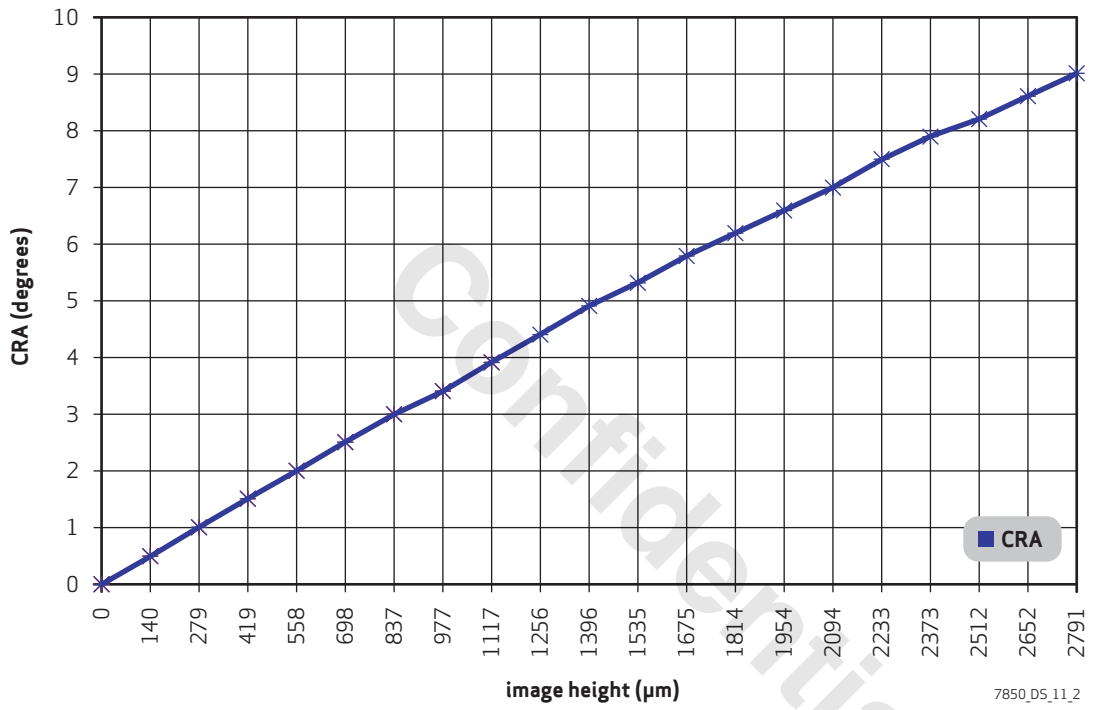

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table 11-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (µm)	CRA (degrees)
0.00	0	0.0
0.05	140	0.5
0.10	279	1.0
0.15	419	1.5
0.20	558	2.0
0.25	698	2.5
0.30	837	3.0
0.35	977	3.4
0.40	1117	3.9
0.45	1256	4.4

table 11-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (µm)	CRA (degrees)
0.50	1396	4.9
0.55	1535	5.3
0.60	1675	5.8
0.65	1814	6.2
0.70	1954	6.6
0.75	2094	7.0
0.80	2233	7.5
0.85	2373	7.9
0.90	2512	8.2
0.95	2652	8.6
1.00	2791	9.0

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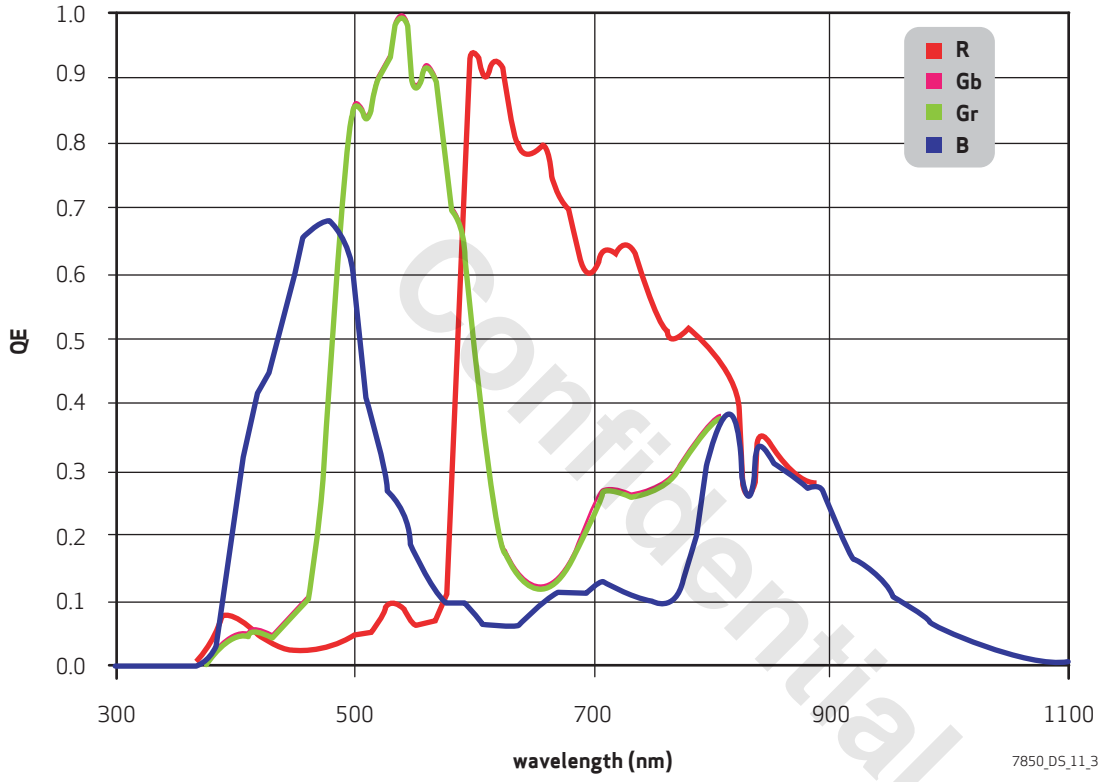
11.3 spectrum response

figure 11-3 spectrum response curve



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appendix A register table

The following table provides a description of the device control registers contained in the OV7850. The 7-bit SCCB slave device address is 0x60 and the low 2 bits can come from GPIO[1:0], which is controlled by 0x300C[0].

In order to guarantee reasonable performance, the initialization register sequence must be based on the register settings provided by OmniVision. Contact your local AE for register settings that suit your application.

table A-1 sensor control registers (sheet 1 of 112)

address	register name	default value	R/W	description
0x3000	PAD_OEN0	0x00	RW	Bit[7:0]: Pad output enable 0
0x3001	PAD_OEN1	0x00	RW	Bit[7:0]: Pad output enable 1
0x3002	PAD_OEN2	0x00	RW	Pad Output Enable 2 Bit[7]: VSYNC output enable Bit[6]: HREF output enable Bit[5]: PCLK output enable Bit[4:3]: Not used
0x3003	PLL_CTRL0	0x24	RW	Bit[7]: pll1_pclk_sel Bit[6:4]: pll1_prediv Bit[3:1]: Reserved Bit[0]: pll1_bypass
0x3004	PLL_CTRL1	0x24	RW	Bit[7:0]: pll1_plldiv
0x3005	PLL_CTRL2	0x51	RW	Bit[7]: pll2_div_rst Bit[6]: pll2_dacdiv Bit[5]: pll1_div_rst Bit[4]: pll1_dacdiv Bit[3:0]: pll1_sysdiv
0x3006	PLL_CTRL3	0x22	RW	Bit[7]: pll2_enable Bit[6:4]: pll2_prediv Bit[3:1]: Reserved Bit[0]: pll2_bypass
0x3007	PCLK_DIV_CTRL	0x00	RW	Bit[7]: Reserved Bit[3:0]: pclk_div
0x3008	PAD_OUT0	0x00	RW	Bit[7:0]: io_y_o[15:8]
0x3009	PAD_OUT1	0x00	RW	Bit[7:0]: io_y_o[7:0]
0x300A	CHIP_ID_H	0xA6	R	Bit[7:0]: Chip ID high byte
0x300B	CHIP_ID_L	0x26	R	Bit[7:0]: Chip ID low byte

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table A-1 sensor control registers (sheet 2 of 112)

address	register name	default value	R/W	description
0x300C	SCCB_ID	0x60	RW	Bit[7:1]: sccb_id_n Bit[0]: sccb_id_sel 0: {sccb_id[7:4],gpio_i[3:1]} 1: sccb_id[7:1]
0x300D	PAD_OUT2	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: io_pclk_o Bit[4:0]: Reserved
0x300E	PAD_SEL0	0x00	RW	Bit[7:0]: io_y_sel[15:8]
0x300F	PAD_SEL1	0x00	RW	Bit[7:0]: io_y_sel[7:0]
0x3010	PAD_SEL2	0x00	RW	Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: io_pclk_sel Bit[4:0]: Reserved
0x3011	A_PAD_PK	0x02	RW	Bit[7:6]: Ip2x3v 00: 1x driving capability 01: 2x driving capability 10: 3x driving capability 11: 4x driving capability Bit[5:3]: Not used Bit[2]: pll_rst 0: Release PLL reset 1: Reset PLLs Bit[1:0]: Not used
0x3012	SENSOR_GATE_ CTRL_H	0xFF	RW	Bit[7]: Sensor gate BLC enable Bit[6]: Sensor gate ISP enable Bit[5]: Sensor gate ISP2X enable Bit[4]: Sensor gate VFIFO enable Bit[3]: Sensor gate DVP enable Bit[2:1]: Not used Bit[0]: Sensor gate OTP enable
0x3013	SREG19	0x08	RW	Bit[7:6]: Not used Bit[5]: Color bar swap order of colors Bit[4]: Color bar enable overlay on output image Bit[3:0]: Color bar amplitude adjustment
0x3016~ 0x3023	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x3024	CORE_CTRL1_H	0x80	RW	Bit[7]: Enables YUV in 8-bit mode Bit[6:4]: raw_modes 000: RAW 10 bits 001: RAW 8 bits 010: RAW 16 bits 100: RAW 18 bits 110: RAW 20 bits Bit[3:0]: Not used
0x3025	CORE_CTRL1_L	0x00	RW	Bit[7:6]: Not used Bit[5]: fsin_out 0: Not used 1: Sensor generated frame sync goes to pad FSIN Bit[4]: c_fsin 0: Pad is input (FSIN) 1: Pad FSIN is output Bit[3:1]: Not used Bit[0]: en_arb0_timeout
0x3029	SUB_ID	–	R	Chip Subversion ID
0x302A~ 0x302E	RSVD	–	–	Reserved
0x302F	GPIO01	0x22	RW	Bit[7]: gpio1_out Bit[6]: gpio1_dir Bit[5:4]: gpio1_sel Bit[3]: gpio0_out Bit[2]: gpio0_dir Bit[1:0]: gpio0_sel
0x3030~ 0x3034	RSVD	–	–	Reserved
0x3035	PLL_CTRL4	0x1C	RW	Bit[7:0]: PLL control
0x3036	GPIO01_2	–	R	Bit[7:5]: Reserved Bit[4]: gpio0_in (read only) Bit[3:1]: Reserved Bit[0]: gpio1_in (read only)
0x3038	MAN_ID_H	–	R	Bit[7:0]: Manufacture ID high byte
0x3039	MAN_ID_L	–	R	Bit[7:0]: Manufacture ID low byte
0x303A	SLP_CNT_H	–	R	SLP_CNT_H
0x303B	SLP_CNT_L	–	R	SLP_CNT_L

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address	register name	default value	R/W	description
0x303E	SOFTWARE_CTRL1	0x00	RW	Bit[7:5]: Not used Bit[4:1]: Reserved Bit[0]: sfw_stb 0: Software standby 1: Streaming
0x303F	SOFTWARE_CTRL2	0x04	RW	Bit[7:3]: Not used Bit[2]: Power down standby option 0: Power down system with software standby 1: Power down system without software standby Bit[1]: Software standby immediately when this bit is set Bit[0]: Software reset
0x3040~ 0x3048	RSVD	–	–	Reserved
0x3105	PWDN_CTRL_SOC	0x03	RW	Bit[7:4]: Not used Bit[3]: early_pll 0: Turn PLL off in software standby 1: Turn PLL on in software standby Bit[2]: early_ana 0: Turn analog off in software standby 1: Turn analog on in software standby Bit[1:0]: Reserved
0x3200	GROUP_LENGTH0	0xFF	RW	Bit[7:0]: Number of registers for group 0, total sum of 4 groups is limited to 768
0x3201	GROUP_LENGTH1	0xFF	RW	Bit[7:0]: Number of registers for group 1
0x3202	GROUP_LENGTH2	0x81	RW	Bit[7:0]: Number of registers for group 2
0x3203	GROUP_LENGTH3	0x81	RW	Bit[7:0]: Number of registers for group 3

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address	register name	default value	R/W	description
0x3204	GROUP_CTRL	0x13	RW	Bit[7]: Hold register writes Bit[6]: Launch immediately, when single_start is set Bit[5]: Launch before sensor core SOF, if single_start is set Bit[4]: Launch after sensor core SOF, if single_start is set Bit[3:2]: Main group select for hold and launch operation (also used as first group in auto mode) 00: Group select 0 01: Group select 1 10: Group select 2 11: Group select 3 Bit[1:0]: Used as second group in auto mode
0x3205	FIRST_GRP_FRAMES	0x01	RW	Bit[7:0]: Frames for staying in group selected by first group selected
0x3206	SECOND_GRP_ FRAMES	0x01	RW	Bit[7:0]: Frames for staying in group selected by second group selected
0x3207	OPERATION_CTRL	0x02	RW	Bit[7:2]: Not used Bit[1]: Auto mode Bit[0]: Single start
0x3208	ACTIVE_GROUP_NR	–	R	Bit[7:2]: Not used Bit[1:0]: Indicates which group is active
0x3209	FRAME_CNT_ACTIVE	–	R	Bit[7:0]: Number of frames with current group (valid only in auto mode)
0x320A	EMB_START_ADDR0_H	0x0F	RW	Bit[7:0]: High address for first embedded data range 0
0x320B	EMB_START_ADDR0_L	0x30	RW	Bit[7:0]: Low address for first embedded data range 0
0x320C	EMB_END_ADDR0_H	0x0F	RW	Bit[7:0]: High address for last embedded data range 0
0x320D	EMB_END_ADDR0_L	0xBF	RW	Bit[7:0]: Low address for last embedded data range 0
0x320E	EMB_START_ADDR1_H	0x40	RW	Bit[7:0]: High address for first embedded data range 1 Change to FF if not used
0x320F	EMB_START_ADDR1_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 1 Change to FF if not used
0x3210	EMB_END_ADDR1_H	0x40	RW	Bit[7:0]: High address for last embedded data range 1

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address	register name	default value	R/W	description
0x3211	EMB_END_ADDR1_L	0x3B	RW	Bit[7:0]: Low address for last embedded data range 1
0x3212	EMB_START_ADDR2_H	0x38	RW	Bit[7:0]: High address for first embedded data range 2 Change to FF if not used
0x3213	EMB_START_ADDR2_L	0x00	RW	Bit[7:0]: Low address for first embedded data range 2 Change to FF if not used
0x3214	EMB_END_ADDR2_H	0x38	RW	Bit[7:0]: High address for last embedded data range 2
0x3215	EMB_END_ADDR2_L	0x8D	RW	Bit[7:0]: Low address for last embedded data range 2
0x3216	EMB_START_ADDR3_H	0xFF	RW	Bit[7:0]: High address for first embedded data range 3 Change to FF if not used
0x3217	EMB_START_ADDR3_L	0xFF	RW	Bit[7:0]: Low address for first embedded data range 3 Change to FF if not used
0x3218	EMB_END_ADDR3_H	0x36	RW	Bit[7:0]: High address for last embedded data range 3
0x3219	EMB_END_ADDR3_L	0x1F	RW	Bit[7:0]: Low address for last embedded data range 3
0x3220	FORCE_BUS_DELAY	0x0C	RW	Bit[7:4]: Not used Bit[3:0]: In module embedded data, delay from start of early VSYNC until register is forced busy
0x3500	R_EXP_L_H	0x00	RW	Bit[7:0]: Long exposure value[15:8]
0x3501	R_EXP_L_L	0x80	RW	Bit[7:0]: Long exposure value[7:0]
0x3502	R_EXP_S_H	0x00	RW	Bit[7:0]: Short exposure value[15:8]
0x3503	R_EXP_S_L	0x50	RW	Bit[7:0]: Short exposure value[7:0]
0x3504	R_EXP_VS	0x2A	RW	Bit[7]: Not used Bit[6:0]: Very short exposure value (xxyyyyy format)
0x3505	R_ANA_GAIN_L	0x00	RW	Bit[7]: Conversion gain 0: Low 1: High Bit[6:0]: Not used
0x3506	R_ANA_GAIN_S	0x00	RW	Bit[7]: Not used Bit[6:0]: Mode 0 short analog gain

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address	register name	default value	R/W	description
0x3507	R_ANA_GAIN_VS	0x00	RW	Bit[7:0]: Mode 0 very short analog gain
0x3508	R_REAL_GAIN_L_H	0x01	RW	Bit[7]: Not used Bit[6:0]: Long exposure real gain[11:5] (integer part)
0x3509	R_REAL_GAIN_L_L	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Long exposure real gain[4:0] (fraction part)
0x350A	R_REAL_GAIN_S_H	0x01	RW	Bit[7]: Not used Bit[6:0]: Short exposure real gain[11:5] (integer part)
0x350B	R_REAL_GAIN_S_L	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Short exposure real gain[4:0] (fraction part)
0x350C	R_REAL_GAIN_VS_H	0x01	RW	Bit[7]: Not used Bit[6:0]: Very short exposure real gain[11:5] (integer part)
0x350D	R_REAL_GAIN_VS_L	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Very short exposure real gain[4:0] (fraction part)
0x350E	R_DIG_GAIN_L_H	0x02	RW	Bit[7:0]: Long exposure digital gain (7+9)[15:8]
0x350F	R_DIG_GAIN_L_L	0x00	RW	Bit[7:0]: Long exposure digital gain (7+9)[7:0]
0x3510	R_DIG_GAIN_S_H	0x02	RW	Bit[7:0]: Short exposure digital gain (7+9)[15:8]
0x3511	R_DIG_GAIN_S_L	0x00	RW	Bit[7:0]: Short exposure digital gain (7+9)[7:0]
0x3512	R_DIG_GAIN_VS_H	0x02	RW	Bit[7:0]: Very short exposure digital gain (7+9)[15:8]
0x3513	R_DIG_GAIN_VS_L	0x00	RW	Bit[7:0]: Very short exposure digital gain (7+9)[7:0]
0x3514	R_AEC_FRAME	0x01	RW	Bit[7:2]: Not used Bit[1]: AEC/AGC change frame flag
0x3515	R_SNR_BLC_L_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC of long exposure[9:8] for sensor core
0x3516	R_SNR_BLC_L_L	0x10	RW	Bit[7:0]: Target BLC of long exposure[7:0] for sensor core

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address	register name	default value	R/W	description
0x3517	R_SNR_BLC_S_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC of short exposure[9:8] for sensor core
0x3518	R_SNR_BLC_S_L	0x10	RW	Bit[7:0]: Target BLC of short exposure[7:0] for sensor core
0x3519	R_SNR_BLC_VS_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC of very short exposure[9:8] for sensor core
0x351A	R_SNR_BLC_VS_L	0x10	RW	Bit[7:0]: Target BLC of very short exposure[7:0] for sensor core
0x3800	CROP_H_ST_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Start address horizontal[9:8]
0x3801	CROP_H_ST_L	0x40	RW	Bit[7:0]: Start address horizontal[7:0]
0x3802	CROP_V_ST_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Start address vertical[9:8]
0x3803	CROP_V_ST_L	0x22	RW	Bit[7:0]: Start address vertical[7:0]
0x3804	CROP_H_END_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: End address horizontal[9:8]
0x3805	CROP_H_END_L	0xCB	RW	Bit[7:0]: End address horizontal[7:0]
0x3806	CROP_V_END_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: End address vertical[9:8]
0x3807	CROP_V_END_L	0x11	RW	Bit[7:0]: End address vertical[7:0]
0x3808	DVP_H_SIZE_H	0x02	RW	Bit[7:0]: DVP horizontal size[15:8]
0x3809	DVP_H_SIZE_L	0x88	RW	Bit[7:0]: DVP horizontal size[7:0]
0x380A	DVP_V_SIZE_H	0x01	RW	Bit[7:0]: DVP vertical size[15:8]
0x380B	DVP_V_SIZE_L	0xE8	RW	Bit[7:0]: DVP vertical size[7:0]
0x380C	HTS_H	0x03	RW	Bit[7:0]: Line length[15:8]
0x380D	HTS_L	0xE9	RW	Bit[7:0]: Line length[7:0]
0x380E	VTS_H	0x02	RW	Bit[7:0]: Frame length[15:8]
0x380F	VTS_L	0x0D	RW	Bit[7:0]: Frame length[7:0]
0x3810	WIN_HOFFS_H	0x00	RW	WIN_HOFFS_H
0x3811	WIN_HOFFS_L	0x08	RW	WIN_HOFFS_L
0x3812	WIN_VOFFS_H	0x00	RW	WIN_VOFFS_H

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address	register name	default value	R/W	description
0x3813	WIN_VOFFS_L	0x04	RW	WIN_VOFFS_L
0x3814	RSVD	–	–	Reserved
0x3815	MIN_REQ_TIME_L	0x90	RW	Bit[7:0]: Minimum time use in sequencer[7:0]
0x3816	EXTRA_DELAY_H	0x00	RW	Bit[7:0]: Last row can be extended by this number
0x3817	EXTRA_DELAY_L	0x00	RW	Bit[7:0]: Last row can be extended by this number
0x3818	SENSOR_CTRL	0x00	RW	Bit[7:5]: Reserved Bit[4]: fsin_en When high, FSIN mode is enabled Bit[3:0]: Reserved
0x3819~ 0x381A	RSVD	–	–	Reserved
0x381B	ABC_FLAG	0x00	RW	Bit[7:2]: Not used Bit[1:0]: abc_flag 00: A 01: B 10: C 11: Not used
0x381C	READ_MODE	0x00	RW	Bit[7:5]: hdr_mode 000: hdr_3exp 001: ls_2exp 010: lvs_2exp 011: l_1exp 100: traffic_3exp Bit[4]: Not used Bit[3]: Flip Bit[2]: Mirror Bit[1]: Vsub2 Bit[0]: Hsub2
0x381D	READ_CTRL	0x04	RW	Bit[7:3]: Not used Bit[2]: show_embedded_rows Bit[1]: show_test_rows Bit[0]: show_black_rows
0x381E~ 0x384F	RSVD	–	–	Reserved
0x3850	A_DAC	0x00	RW	Bit[7:6]: Not used Bit[5:0]: NTSC DAC control
0x3851	A_REGULATOR	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Voltage regulator control

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address	register name	default value	R/W	description
0x3852	A_TPM	0x00	RW	Bit[7:5]: Not used Bit[4]: Disable temperature monitor Bit[3:0]: a_tpm_ctrl
0x3853	A_BOD_H	0x02	RW	Bit[7:5]: Not used Bit[4:0]: brown_out control[12:8]
0x3854	A_BOD_L	0x10	RW	Bit[7:0]: brown_out control[7:0]
0x3880	EXPOSURE_LONG_H	–	R	Bit[7:0]: Frame long exposure (in rows)[15:8]
0x3881	EXPOSURE_LONG_L	–	R	Bit[7:0]: Frame long exposure (in rows)[7:0]
0x3882	EXPOSURE_SHORT_H	–	R	Bit[7:0]: Frame short exposure (in rows)[15:8]
0x3883	EXPOSURE_SHORT_L	–	R	Bit[7:0]: Frame short exposure (in rows)[7:0]
0x3884	EXPOSURE_VERY_ SHORT	–	R	Bit[7]: Not used Bit[6:0]: Frame very short exposure (in rows), form
0x3885	GROUP_HIT	–	R	Bit[7:4]: Not used Bit[3:0]: group_hit
0x3886	FCNT_H	–	R	FCNT_H
0x3887	FCNT_L	–	R	FCNT_L
0x3888~ 0x388C	RSVD	–	–	Reserved
0x388D	ABC_MODE_CURRENT	–	R	Bit[7:2]: Not used Bit[1:0]: Mode for current frame
0x3D00	OTP_BYTE0	0x00	RW	OTP Write/read Buffer 0
0x3D01	OTP_BYTE1	0x00	RW	OTP Write/read Buffer 1
0x3D02	OTP_BYTE2	0x00	RW	OTP Write/read Buffer 2
0x3D03	OTP_BYTE3	0x00	RW	OTP Write/read Buffer 3
0x3D04	OTP_BYTE4	0x00	RW	OTP Write/read Buffer 4
0x3D05	OTP_BYTE5	0x00	RW	OTP Write/read Buffer 5
0x3D06	OTP_BYTE6	0x00	RW	OTP Write/read Buffer 6
0x3D07	OTP_BYTE7	0x00	RW	OTP Write/read Buffer 7
0x3D08	OTP_BYTE8	0x00	RW	OTP Write/read Buffer 8
0x3D09	OTP_BYTE9	0x00	RW	OTP Write/read Buffer 9

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address	register name	default value	R/W	description
0x3D0A	OTP_BYTE10	0x00	RW	OTP Write/read Buffer 10
0x3D0B	OTP_BYTE11	0x00	RW	OTP Write/read Buffer 11
0x3D0C	OTP_BYTE12	0x00	RW	OTP Write/read Buffer 12
0x3D0D	OTP_BYTE13	0x00	RW	OTP Write/read Buffer 13
0x3D0E	OTP_BYTE14	0x00	RW	OTP Write/read Buffer 14
0x3D0F	OTP_BYTE15	0x00	RW	OTP Write/read Buffer 15
0x3D80	R_PGM_CTR	0x00	RW	Bit[7:1]: Not used Bit[0]: otp_pgm Program start signal Writing 1 to this register starts programing
0x3D81	R_LOAD_CTR	0x00	RW	Bit[7:1]: Not used Bit[0]: otp_rd Read start signal Writing 1 to this register starts loading data
0x3D82	R_PGM_PULSE	0x40	RW	Bit[7:0]: Program pulse Control load strobe pulse by Tsclk
0x3D83	R_LOAD_PULSE	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Load pulse Control load strobe pulse by Tsclk
0x3D84	R_MODE_CTRL	0x40	RW	Bit[7]: program_dis 1: Disable programming Bit[6]: mode_select 0: Auto mode 1: Manual mode Bit[5:0]: Choose bank in OTP 0: Bank 0 1: Bank 1
0x3D85	R_START_ADDRESS	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Start address for manual mode
0x3D86	R_END_ADDRESS	0x0F	RW	Bit[7:4]: Not used Bit[3:0]: End address for manual mode
0x3D87	R_PS2CS	0x03	RW	Bit[7:4]: Not used Bit[3:0]: PS to CSB time control, by sclk
0x3D88	LD_WR_GAP	0x08	RW	Bit[7:0]: Load write register gap
0x3D89	LOAD_CTRL	0x00	RW	Bit[7:0]: OTP load setting enable

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address	register name	default value	R/W	description
0x3D8A	R_OTP_PROG_O	–	R	Bit[7:1]: Not used Bit[0]: otp_prog_o 1: Programming
0x3D8B	R_OTP_LOAD_O	–	R	Bit[7:1]: Not used Bit[0]: otp_load_o 1: Loading
0x4000	BLC_CTRL0	0x75	RW	Bit[7]: Not used Bit[6]: Enable dig_offset_corr_s, S exposure When not enabled, register value will be used Bit[5]: Enable adc_offset_corr_s, S exposure When not enabled, register value will be used Bit[4]: Enable dac_offset_corr_s, S exposure When not enabled, register value will be used Bit[3]: Not used Bit[2]: Enable dig_offset_corr_l, L exposure When not enabled, register value will be used Bit[1]: Enable adc_offset_corr_l, L exposure When not enabled, register value will be used Bit[0]: Enable dac_offset_corr_l, L exposure When not enabled, register value will be used
0x4001	BLC_CTRL1	0x17	RW	Bit[7:5]: Not used Bit[4]: en_retrig_offset_change Bit[3]: Disable adc_corr_logic Used for test and debugging Bit[2]: Enable dig_offset_corr_vs, VS exposure When not enabled, register value will be used Bit[1]: Enable adc_offset_corr_vs, VS exposure When not enabled, register value will be used Bit[0]: Enable dac_offset_corr_vs, VS exposure When not enabled, register value will be used

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address	register name	default value	R/W	description
0x4002	BLC_MODE	0x0E	RW	Bit[7]: Output filtered values of BLC calculations if enabled Bit[6]: Enable manual target adjustment from registers Bit[5]: Restart BLC Bit[4]: Enable automatic temperature change re-trigger Bit[3]: Enable automatic exposure change re-trigger Bit[2]: Enable automatic gain change re-trigger Bit[1]: Filter mode 1/4 new + 3/4 old value, affecting only dig_offset_corr Bit[0]: Updates every frame
0x4003	RESTART_FRAMES	0x01	RW	Bit[7:0]: Number of frames with continuous update after restart
0x4005	DAC_OFFSET_R_L	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Use this value for L exposure, when dac_offset_corr is disabled
0x4005	BLC CTRL05	0x18	RW	Bit[7:5]: Not used Bit[4]: Optical black row output disable 0: Output optical black rows in image 1: Do not output optical black row Bit[2]: Reverse red-blue row indicator for BLC Bit[1:0]: Not used
0x4006	DAC_OFFSET_R_S	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Use this value for S exposure, when dac_offset_corr is disabled
0x4007	DAC_OFFSET_R_VS	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Use this value for VS exposure, when dac_offset_corr is disabled
0x4008	ADC_OFFSET_R_L	0x00	RW	Bit[7]: Not used Bit[6:0]: Use this value for L exposure, when adc_offset_corr is disabled
0x4009	ADC_OFFSET_R_S	0x00	RW	Bit[7]: Not used Bit[6:0]: Use this value for S exposure, when adc_offset_corr is disabled
0x400A	ADC_OFFSET_R_VS	0x00	RW	Bit[7]: Not used Bit[6:0]: Use this value for VS exposure, when adc_offset_corr is disabled

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address	register name	default value	R/W	description
0x400B	DIG_OFFSET_R_L	0x00	RW	Bit[7:0]: Use this value for L exposure, when dig_offset_corr is disabled
0x400C	DIG_OFFSET_R_S	0x00	RW	Bit[7:0]: Use this value for S exposure, when dig_offset_corr is disabled
0x400D	DIG_OFFSET_R_VS	0x00	RW	Bit[7:0]: Use this value for VS exposure, when dig_offset_corr is disabled
0x400E	BLC_TARGET_MAN_L_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: BLC target for L exposure when not in ISP mode[9:8] (manual_target_enable=1)
0x400F	BLC_TARGET_MAN_L_L	0x00	RW	Bit[7:0] BLC target for L exposure when not in ISP mode[7:0] (manual_target_enable=1)
0x4010	BLC_TARGET_MAN_S_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: BLC target for S exposure when not in ISP mode[9:8] (manual_target_enable=1)
0x4011	BLC_TARGET_MAN_S_L	0x00	RW	Bit[7:0]: BLC target for S exposure when not in ISP mode[7:0] (manual_target_enable=1)
0x4012	BLC_TARGET_MAN_ VS_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: BLC target for VS exposure when not in ISP mode[9:8] (isp_mode_n=1)
0x4013	BLC_TARGET_MAN_ VS_L	0x00	RW	Bit[7:0]: BLC target for VS exposure when not in ISP mode[7:0] (isp_mode_n=1)
0x4014	DARK_CURRENT_L_H	–	R	Bit[7:2]: Not used Bit[1:0]: Measured dark current for L exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4015	DARK_CURRENT_L_L	–	R	Bit[7:0]: Measured dark current for L exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4016	DARK_CURRENT_S_H	–	R	Bit[7:2]: Not used Bit[1:0]: Measured dark current for S exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter

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address	register name	default value	R/W	description
0x4017	DARK_CURRENT_S_L	–	R	Bit[7:0]: Measured dark current for S exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4018	DARK_CURRENT_VS_H	–	R	Bit[7:2]: Not used Bit[1:0]: Measured dark current for VS exposure[9:8] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x4019	DARK_CURRENT_VS_L	–	R	Bit[7:0]: Measured dark current for VS exposure[7:0] Filter mode (1/4 new, 3/4 old) Re-trigger overrides filter
0x401A	ROW_AVERAGE_01_L_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 0 and 1[11:8] L exposure, filter mode (1/4 new, 3/4 old), re-trigger overrides filter
0x401B	ROW_AVERAGE_01_L_L	–	R	Bit[7:0]: Average value for rows 0 and 1[7:0] L exposure, filter mode (1/4 new, 3/4 old), re-trigger overrides filter
0x401C	ROW_AVERAGE_01_S_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 0 and 1[11:8] S exposure
0x401D	ROW_AVERAGE_01_S_L	–	R	Bit[7:0]: Average value for rows 0 and 1[7:0] S exposure
0x401E	ROW_AVERAGE_01_VS_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 0 and 1[11:8] VS exposure
0x401F	ROW_AVERAGE_01_VS_L	–	R	Bit[7:0]: Average value for rows 0 and 1[7:0] VS exposure
0x4020	ROW_AVERAGE_23_L_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 2 and 3[11:8] L exposure
0x4021	ROW_AVERAGE_23_L_L	–	R	Bit[7:0]: Average value for rows 2 and 3[7:0] L exposure
0x4022	ROW_AVERAGE_23_S_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 2 and 3[11:8] S exposure
0x4023	ROW_AVERAGE_23_S_L	–	R	Bit[7:0]: Average value for rows 2 and 3[7:0] S exposure

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address	register name	default value	R/W	description
0x4024	ROW_AVERAGE_23_ VS_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 2 and 3[11:8] VS exposure
0x4025	ROW_AVERAGE_23_ VS_L	–	R	Bit[7:0]: Average value for rows 2 and 3[7:0] VS exposure
0x4026	ROW_AVERAGE_45_L_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 4 and 5[11:8] L exposure
0x4027	ROW_AVERAGE_45_L_L	–	R	Bit[7:0]: Average value for rows 4 and 5[7:0] L exposure
0x4028	ROW_AVERAGE_45_S_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 4 and 5[11:8] S exposure
0x4029	ROW_AVERAGE_45_S_L	–	R	Bit[7:0]: Average value for rows 4 and 5[7:0] S exposure
0x402A	ROW_AVERAGE_45_ VS_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 4 and 5[11:8] VS exposure
0x402B	ROW_AVERAGE_45_ VS_L	–	R	Bit[7:0]: Average value for rows 4 and 5[7:0] VS exposure
0x402C	ROW_AVERAGE_67_L_H	–	R	Bit[7:4]: Not used Bit[3:0] Average value for rows 6 and 7[11:8] L exposure
0x402D	ROW_AVERAGE_67_L_L	–	R	Bit[7:0]: Average value for rows 6 and 7[7:0] L exposure
0x402E	ROW_AVERAGE_67_S_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 6 and 7[11:8] S exposure
0x402F	ROW_AVERAGE_67_S_L	–	R	Bit[7:0]: Average value for rows 6 and 7[7:0] S exposure
0x4030	ROW_AVERAGE_67_ VS_H	–	R	Bit[7:4]: Not used Bit[3:0]: Average value for rows 6 and 7[11:8] VS exposure
0x4031	ROW_AVERAGE_67_ VS_L	–	R	Bit[7:0]: Average value for rows 6 and 7[7:0] VS exposure
0x4032	DAC_OFFSET_STEP	0x0D	RW	Bit[7:0]: DAC offset step
0x4033	DAC_OFFSET_BIAS	0x14	RW	Bit[7:0]: DAC offset bias Subtracted before division

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address	register name	default value	R/W	description
0x4034	CLK_RATIO	0x80	RW	Bit[7:0]: Ratio (ADC_CLK×2)/(SCLK3X) format 3.5
0x4035	D_VALUE_L_VS	0x00	RW	Bit[7:6]: Not used Bit[5]: Sign (S) Bit[4:0]: Value (xyzuv) -/+ (S) 0.0x40yzuv is used to equalize dark current for visual and dark pixels
0x4036	D_VALUE_S	0x00	RW	Bit[7:6]: Not used Bit[5]: Sign (S) Bit[4:0]: Value (xyzuv) -/+ (S) 0.0x40yzuv is used to equalize dark current for visual and dark pixels
0x4037	OFFSET_THRES_L	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x4038	OFFSET_THRES_S	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x4039	OFFSET_THRES_VS	0x20	RW	Bit[7:0]: When enabled, if dig offset changes by this value, BLC will re-trigger
0x403A	N_TARGET_BIAS_L	0x00	RW	Bit[7:0]: Bias for ADC offset L
0x403B	N_TARGET_BIAS_S	0x00	RW	Bit[7:0]: Bias for ADC offset S
0x403C	N_TARGET_BIAS_VS	0x00	RW	Bit[7:0]: Bias for ADC offset VS
0x4040	VARIANCE_L_H	–	R	Bit[7:0]: Variance dark current, L exposure[15:8]
0x4041	VARIANCE_L_L	–	R	Bit[7:0]: Variance dark current, L exposure[7:0]
0x4042	VARIANCE_S_H	–	R	Bit[7:0]: Variance dark current, S exposure[15:8]
0x4043	VARIANCE_S_L	–	R	Bit[7:0]: Variance dark current, S exposure[7:0]
0x4044	VARIANCE_VS_H	–	R	Bit[7:0]: Variance dark current, VS exposure[15:8]
0x4045	VARIANCE_VS_L	–	R	Bit[7:0]: Variance dark current, VS exposure[7:0]
0x4046	COL_AMP_OFS_L	–	R	Bit[7:5]: Not used Bit[4:0]: BLC calculated DAC value for L exposure
0x4047	COL_AMP_OFS_S	–	R	Bit[7:5]: Not used Bit[4:0]: BLC calculated DAC value for S exposure

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address	register name	default value	R/W	description
0x4048	COL_AMP_OFS_VS	–	R	Bit[7:5]: Not used Bit[4:0]: BLC calculated DAC value for VS exposure
0x4049	N_TARGET_L	–	R	Bit[7:0]: BLC calculated ADC correction value for L exposure
0x404A	N_TARGET_S	–	R	Bit[7:0]: BLC calculated ADC correction value for S exposure
0x404B	N_TARGET_VS	–	R	Bit[7:0]: BLC calculated ADC correction value for VS exposure
0x404C	DIG_OFFSET_L	–	R	Bit[7:0]: BLC calculated digital offset value for L exposure
0x404D	DIG_OFFSET_S	–	R	Bit[7:0]: BLC calculated digital offset value for S exposure
0x404E	DIG_OFFSET_VS	–	R	Bit[7:0]: BLC calculated digital offset value for VS exposure
0x4200	FCNT_CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: Reserved Bit[2]: Fcnt EOF select Bit[1]: Fcnt mask disable Bit[0]: Fcnt reset
0x4201	FRAME_ON_NUMBER	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Frame on number
0x4202	FRAME_OFF_NUMBER	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Frame off number
0x4203	MASK_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Rblue mask disable Bit[5]: Data mask disable Bit[4]: Valid mask disable Bit[3]: HREF mask disable Bit[2]: EOF mask disable Bit[1]: SOF mask disable Bit[0]: All mask disable
0x4300	CTRL00	0x30	RW	Bit[7:4]: data_type 0000: raw_en 0001: y8_en 0011: yuv422_en 1111: byp_fmt Bit[3:0]: Pixel order control 0000: YUYV 0001: YVYU 0010: UYVY 0011: VYUY

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address	register name	default value	R/W	description
0x4301	CTRL01	0x04	RW	Bit[7:6]: Reserved Bit[5]: Output format option2 for raw_x3 & RAW8 or 8-bit YUV422 Bit[4:3]: raw_type 00: raw_x1 01: raw_x2 1x: raw_x3 Bit[2:0]: raw_sel If raw_type == raw_x1: 000: {data1} 001: {data2} 010: {data3} If raw_type == raw_x2: 000: {data1,data2} 001: {data2,data3} 010: {data1,data3} 100: {data2,data1} 101: {data3,data2} 110: {data3,data1} If raw_type == raw_x3: 000: {data1,data2,data3} 001: {data1,data3,data2} 010: {data2,data1,data3} 011: {data2,data3,data1} 100: {data3,data1,data2} 101: {data3,data2,data1}
0x4302~ 0x4309	RSVD	–	–	Reserved
0x4700	MOD_SEL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Ccir656_blank_seq H-blank data toggle sequence 0: 80,10 1: 10,80 Bit[4:3]: Reserved Bit[2]: ccir656_f_value 0: 656's sync code fixed at field 0 1: 656's sync code fixed at field 1 Bit[1]: ccir656_mode_enable Bit[0]: Reserved
0x4701	LONG VSYNC MODE	0x00	RW	Bit[7:1]: Not used Bit[0]: Long VSYNC mode 0: Disable 1: Enable
0x4702	VSYNC_WIDTH_LINE_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: VSYNC width by line number[9:8]
0x4703	VSYNC_WIDTH_LINE_L	0x00	RW	Bit[7:0]: VSYNC width by line number[7:0]

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address	register name	default value	R/W	description
0x4704	VSYNC_WIDTH_PIXEL_H	0x02	RW	Bit[7:0]: VSYNC width by pixel number[15:8]
0x4705	VSYNC_WIDTH_PIXEL_L	0x00	RW	Bit[7:0]: VSYNC width by pixel number[7:0]
0x4706	VSYNC_MODE	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Reserved
0x4707	VSYNC_DELAY_H	0x00	RW	Bit[7:0]: VSYNC delay count[23:16]
0x4708	VSYNC_DELAY_M	0x00	RW	Bit[7:0]: VSYNC delay count[15:8]
0x4709	VSYNC_DELAY_L	0x00	RW	Bit[7:0]: VSYNC delay count[7:0]
0x470A	POLARITY_CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: Bit reverse enable Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: Reserved Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity also PCLK gate low enable
0x470B	WALKING_1_TEST_PATTERN	0x00	RW	Bit[7]: Reserved Bit[6:4]: DVP data bit swap option Bit swap selection 1 (byp_select[5] = 0): 000: D[15:0] 001: D[0:15] 010: D[2:15], D[1:0] 011: D[4:15], D[3:0] 100: D[6:15], D[0:5] 101: D[8:15], D[0:7] 110: D[10:15], D[0:9] 111: D[12:15], D[0:11] Bit swap selection 2 (byp_select[5] = 1): 000: D[13:0], D[15:14] 001: D[11:0], D[15:12] 010: D[9:0], D[15:10] 011: D[7:0], D[15:8] 100: D[5:0], D[15:6] 101: D[3:0], D[15:4] 110: D[1:0], D[15:2] 111: 16'h0 Bit[3]: test_mode Bit[2]: test_bit10 Bit[1]: test_bit8 Bit[0]: test_enable

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address	register name	default value	R/W	description
0x470C	BYP_SELECT	0x00	RW	Bit[7:6]: Not used Bit[5]: Choose DVP data bit swap selection in register 0x470B[6:4] 0: Bit swap selection 1 1: Bit swap selection 2 Bit[4]: href_sel Bit[3:0]: bypass_sel
0x470D	BYP_CTRL2	0x00	RW	Bit[7:6]: Not used Bit[5]: bypass_pclk Bit[4]: bypass_href Bit[3]: bypass_vsync Bit[2:0]: Bypass data[15:13]
0x470E	BYP_CTRL1	0x00	RW	Bit[7.0]: Bypass data[12:5]
0x470F	BYP_CTRL0	0x00	RW	Bit[7:3]: Bypass data[4:0] Bit[2]: bypass_gpio1 (sck pin) Bit[1]: bypass_gpio2 (sd_o pin) Bit[0]: bypass_gpio3 (sd_i pin)
0x4710	RSVD	–	–	Reserved
0x4800	CVBS_CTRL_H	0x22	RW	Bit[7]: Test pattern Bit[6]: Progressive mode Bit[5]: Field option Bit[4]: Low pass filter enable Bit[3]: Reserved Bit[2]: Fixed phase Bit[1]: XSYNC option Bit[0]: PAL mode
0x4801	CVBS_CTRL_L	0x00	RW	Bit[7]: Oversample option, double sample DAC data Bit[6]: 27MHz system clock option Bit[5]: Reserved Bit[4]: YCbCr correction enable Bit[3]: NTSC 433 mode Bit[2]: Fixed DAC data enable Bit[1]: VSYNC option to reset TV timing Bit[0] Reserved
0x4802	FIX_DATA_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Fixed data output[9:8] When fixdata_en =1 (0x4801[2]), tvenc will output fixed data
0x4803	FIX_DATA_L	0x00	RW	Bit[7:0]: Fixed data output[7:0] When fixdata_en =1 (0x4801[2]), tvenc will output fixed data

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address	register name	default value	R/W	description
0x4804	SCALING	0x00	RW	Bit[7:3]: Not used Bit[2]: FIFO read timing option, should be fixed in one project Bit[1:0]: Xscale option
0x4810	XSXOFFSET_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: X offset[12:8] Point on sensor timing domain to start TV timing counter
0x4811	XSXOFFSET_L	0x01	RW	Bit[7:0]: X offset[7:0] Point on sensor timing domain to start TV timing counter
0x4812	XSYOFFSET_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Y offset[9:8] Point on sensor timing domain to start TV timing counter
0x4813	XSYOFFSET_L	0x0D	RW	Bit[7:0]: Y offset[7:0] Point on sensor timing domain to start TV timing counter
0x4814	WIDTH_H	0x06	RW	Bit[7:5]: Not used Bit[4:0]: TV output active image width[12:8]
0x4815	WIDTH_L	0x18	RW	Bit[7:0]: TV output active image width[7:0]
0x4816	HEIGHT_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: TV output active image height[9:8]
0x4817	HEIGHT_L	0xE8	RW	Bit[7:0]: TV output active image height[7:0]
0x4820	VSTART1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Active image start line in TV timing field 1 (interlaced mode)[9:8]
0x4821	VSTART1_L	0x13	RW	Bit[7:0]: Active image start line in TV timing field 1 (interlaced mode)[7:0]
0x4822	VSTOP1_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Active image end line in TV timing field 1 (interlaced mode)[9:8]
0x4823	VSTOP1_L	0x07	RW	Bit[7:0] Active image end line in TV timing field 1 (interlaced mode)[7:0]
0x4824	VSTART2_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Active image start line in TV timing field 2 (interlaced mode)[9:8]
0x4825	VSTART2_L	0x1A	RW	Bit[7:0]: Active image start line in TV timing field 2 (interlaced mode)[7:0]

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address	register name	default value	R/W	description
0x4826	VSTOP2_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Active image end line in TV timing field 2 (interlaced mode)[9:8]
0x4827	VSTOP2_L	0x0E	RW	Bit[7:0]: Active image end line in TV timing field 2 (interlaced mode)[7:0]
0x4828	VSTART3_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Active image start line in TV timing (progressive mode)[9:8]
0x4829	VSTART3_L	0x18	RW	Bit[7:0]: Active image start line in TV timing (progressive mode)[7:0]
0x482A	VSTOP3_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Active image end line in TV timing (progressive mode)[9:8]
0x482B	VSTOP3_L	0xF8	RW	Bit[7:0]: Active image end line in TV timing (progressive mode)[7:0]
0x482C	SCSHIFT_3	0x25	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482D	SCSHIFT_2	0x55	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482E	SCSHIFT_1	0x55	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x482F	SCSHIFT_0	0x63	RW	Bit[7:0]: Subcarrier phase adjustment parameter 3
0x4830	WHITELEVEL_H	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Maximum luminance signal level on TV (for 10-bit encoder)[9:8]
0x4831	WHITELEVEL_L	0xFF	RW	Bit[7:0]: Maximum luminance signal level on TV (for 10-bit encoder)[7:0]
0x4832	NORMLEVEL_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Minimum luminance signal level on TV (for 10-bit encoder)[9:8]
0x4833	NORMLEVEL_L	0x1A	RW	Bit[7:0]: Minimum luminance signal level on TV (for 10-bit encoder)[7:0]
0x4834	BLANKLEVEL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Blanking level on TV[9:8]
0x4835	BLANKLEVEL_L	0xF0	RW	Bit[7:0]: Blanking level on TV[7:0]
0x4836	SYNCSTEPS	0x02	RW	Bit[7:0]: Step number when blanking level switching to sync level

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address	register name	default value	R/W	description
0x4837	BURSTSTEPS	0x02	RW	Bit[7:0]: Step number for burst level changing
0x4838	SYNCLEVEL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Sync level on TV[9:8]
0x4839	SYNCLEVEL_L	0x10	RW	Bit[7:0]: Sync level on TV[7:0]
0x483A	BURSTLEVEL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Amplitude of burst on TV[9:8]
0x483B	BURSTLEVEL_L	0x73	RW	Bit[7:0]: Amplitude of burst on TV[7:0]
0x483C	SYNCDELTA_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Syncdelta[9:8] (blank level - sync level) / sync_steps
0x483D	SYNCDELTA_L	0x70	RW	Bit[7:0]: Syncdelta[7:0] (blank level - sync level) / sync_steps
0x483E	BURSTDELTA_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Burstdelta[9:8] Burst level / burst step
0x483F	BURSTDELTA_L	0x38	RW	Bit[7:0]: Burstdelta[7:0] Burst level / burst step
0x4840	HCSYNCON_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of horizontal sync start point[12:8]
0x4841	HCSYNCON_L	0x1D	RW	Bit[7:0]: TV line counter value of horizontal sync start point[7:0]
0x4842	HCSYNCOFF_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of horizontal sync end point[12:8]
0x4843	HCSYNCOFF_L	0x91	RW	Bit[7:0]: TV line counter value of horizontal sync end point[7:0]
0x4844	HCBURSTON_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of burst start point[12:8]
0x4845	HCBURSTON_L	0x9F	RW	Bit[7:0]: TV line counter value of burst start point[7:0]
0x4846	HCBURSTOFF_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of burst end point[12:8]
0x4847	HCBURSTOFF_L	0xDD	RW	Bit[7:0]: TV line counter value of burst end point[7:0]

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address	register name	default value	R/W	description
0x4848	HCACTIVEON_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of active pixel start point[12:8]
0x4849	HCACTIVEON_L	0xFA	RW	Bit[7:0]: TV line counter value of active pixel start point[7:0]
0x484A	HCACTIVEOFF_H	0x06	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of active pixel end point[12:8]
0x484B	HCACTIVEOFF_L	0x0A	RW	Bit[7:0]: TV line counter value of active pixel end point[7:0]
0x484C	HCVALIDON_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of valid start point[12:8]
0x484D	HCVALIDON_L	0xFA	RW	Bit[7:0]: TV line counter value of valid start point[7:0]
0x484E	HCVALIDOFF_H	0x06	RW	Bit[7:5]: Not used Bit[4:0]: TV line counter value of valid end point[12:8]
0x484F	HCVALIDOFF_L	0x0A	RW	Bit[7:0]: TV line counter value of valid end point[7:0]
0x4850	MINLEVEL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Minimum level of DAC input data[9:8]
0x4851	MINLEVEL_L	0x01	RW	Bit[7:0]: Minimum level of DAC input data[7:0]
0x4852	MAXLEVEL_H	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Maximum level of DAC input data[9:8]
0x4853	MAXLEVEL_L	0xFF	RW	Bit[7:0]: Maximum level of DAC input data[7:0]
0x4854~ 0x4857	RSVD	–	–	Reserved
0x4858	CHROMASAT_H	0x01	RW	Bit[7:1]: Not used Bit[0]: Chroma signal saturation level[8]
0x4859	CHROMASAT_L	0xFF	RW	Bit[7:0]: Chroma signal saturation level[7:0]
0x485A	RSVD	–	–	Reserved
0x485B	FETCH_OFFS	0x03	RW	Bit[7:0]: Horizontal FIFO data fetch signal offset

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address	register name	default value	R/W	description
0x4860~ 0x487F	RSVD	–	–	Reserved
0x5000	R_ISP_CTRL_0	0xFB	RW	Bit[7]: AEC/AGC enable Bit[6]: Combine enable Bit[5]: Curve WB/manual WB enable 0: Manual WB enable 1: Curve WB enable Bit[4]: Simple interpolation enable Bit[3]: HDR RAW DNS enable Bit[2]: LENC enable Bit[1]: AWB gain enable Bit[0]: ISP enable
0x5001	R_ISP_CTRL_1	0xDF	RW	Bit[7]: OVPB CIP pad enable Bit[6]: OVPB CIP enable Bit[5]: OVPB RAW DNS enable Bit[4]: Reserved Bit[3]: DPC enable Bit[2]: Linear stretch enable Bit[1]: Log enable Bit[0]: Tone mapping enable
0x5002	R_ISP_CTRL_2	0x7F	RW	Bit[7]: Make virtual long enable Bit[6]: UVDNS enable Bit[5]: HDR statistic enable Bit[4]: ISP sub-module clock global enable Bit[3]: RGB2YUV enable Bit[2]: Reserved Bit[1]: Gamma enable Bit[0]: CMX enable
0x5003	R_ISP_CTRL_3	0xB0	RW	Bit[7]: ISP output window crop enable (active high) Bit[6]: ISP input window crop enable (active high) Bit[5]: OVPB buffer auto dummy line enable Bit[4]: HDR buffer auto dummy line enable Bit[3:2]: ISP EOF signal select Bit[1:0]: CFA pattern
0x5004~ 0x5006	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x5007	R_ISP_CTRL_7	0x00	RW	Bit[7]: ISP output RAW10 selection 0: Non-combined RAW 10 1: Combined RAW10 Bit[6]: Manual sensor option enable Bit[5]: Manual sensor mirror option Bit[4]: Manual sensor flip option Bit[3:2]: Manual sensor X skip Bit[1:0]: Manual sensor Y skip
0x5008	R_ISP_CTRL_8	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual sensor X offset[9:8]
0x5009	R_ISP_CTRL_9	0x00	RW	Bit[7:0]: Manual sensor X offset[7:0]
0x500A	R_ISP_CTRL_A	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual sensor Y offset[9:8]
0x500B	R_ISP_CTRL_B	0x00	RW	Bit[7:0]: Manual sensor Y offset[7:0]
0x500C	R_ISP_CTRL_C	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC for long[9:8]
0x500D	R_ISP_CTRL_D	0x10	RW	Bit[7:0]: Target BLC for long[7:0]
0x500E	R_ISP_CTRL_E	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC for short[9:8]
0x500F	R_ISP_CTRL_F	0x10	RW	Bit[7:0]: Target BLC for short[7:0]
0x5010	R_ISP_CTRL_10	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Target BLC for vshort[9:8]
0x5011	R_ISP_CTRL_11	0x10	RW	Bit[7:0]: Target BLC for vshort[7:0]
0x5012	R_ISP_CTRL_12	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ISP input window crop X direction (horizontal) start coordinate[9:8]
0x5013	R_ISP_CTRL_13	0x00	RW	Bit[7:0]: ISP input window crop X direction (horizontal) start coordinate[7:0]
0x5014	R_ISP_CTRL_14	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ISP input window crop Y direction (vertical) start coordinate[9:8]
0x5015	R_ISP_CTRL_15	0x00	RW	Bit[7:0]: ISP input window crop Y direction (vertical) start coordinate[7:0]
0x5016	R_ISP_CTRL_16	0x02	RW	Bit[7:2]: Not used Bit[1:0]: ISP input window crop module output width[9:8]
0x5017	R_ISP_CTRL_17	0xF0	RW	Bit[7:0]: ISP input window crop module output width[7:0]

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table A-1 sensor control registers (sheet 28 of 112)

address	register name	default value	R/W	description
0x5018	R_ISP_CTRL_18	0x02	RW	Bit[7:2]: Not used Bit[1:0]: ISP input window crop module output height[9:8]
0x5019	R_ISP_CTRL_19	0x08	RW	Bit[7:0]: ISP input window crop module output height[7:0]
0x501A~ 0x501D	RSVD	–	–	Reserved
0x501E	R_ISP_CTRL_1E	0x00	RW	Bit[7]: HDR buffer manual control enable Bit[6]: OVPB buffer manual control enable Bit[5]: HDR buffer manual enable Bit[4]: OVPB buffer manual enable Bit[3:2]: RGB2YUV bypass channel select 00: G channel 01: G channel 10: B channel 11: R channel Bit[1]: HDR buffer control dummy line manual HREF blank cycles enable Bit[0]: OVPB buffer control dummy line manual HREF blank cycles enable
0x501F	R_PRE_CTRL0	0x00	RW	Bit[7]: Test pattern enable (active high) Bit[6]: Rolling effect enable (active high) Bit[5]: Transparent effect enable (active high) Bit[4]: Not used Bit[3:2]: Color bar style select Bit[1:0]: Test pattern select 00: Color bar Others: Not used
0x5020~ 0x50C7	RSVD	–	–	Reserved
0x5080~ 0x5081	AWBRGAIN_L	0x128	RW	Long Channel Red Gain
0x5082~ 0x5083	AWBGRGAIN_L	0x100	RW	Long Channel Gr Gain
0x5084~ 0x5085	AWBGBGAIN_L	0x100	RW	Long Channel Gb Gain
0x5086~ 0x5087	AWBBGAIN_L	0x200	RW	Long Channel Blue Gain
0x5088~ 0x5089	AWBRGAIN_S	0x128	RW	Short Channel Red Gain

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address	register name	default value	R/W	description
0x508A~ 0x508B	AWBGRGAIN_S	0x100	RW	Short Channel Gr Gain
0x508C~ 0x508D	AWBGBGAIN_S	0x100	RW	Short channel Gb Gain
0x508E~ 0x508F	AWBBGAIN_S	0x200	RW	Short channel Blue Gain
0x5090~ 0x5091	AWBRGAIN_VS	0x128	RW	Very Short Channel Red Gain
0x5092~ 0x5093	AWBGRGAIN_VS	0x100	RW	Very Short Channel Gr Gain
0x5094~ 0x5095	AWBGBGAIN_VS	0x100	RW	Very Short Channel Gb Gain
0x5096~ 0x5097	AWBBGAIN_VS	0x200	RW	Very Short Channel Blue Gain
0x5100	R_NOISELIST0_L_I	0x01	RW	Bit[7:0]: NoiseList0 for L exposure channel RAW de-noise
0x5101	R_NOISELIST1_L_I	0x02	RW	Bit[7:0]: NoiseList1 for L exposure channel RAW de-noise
0x5102	R_NOISELIST2_L_I	0x04	RW	Bit[7:0]: NoiseList2 for L exposure channel RAW de-noise
0x5103	R_NOISELIST3_L_I	0x08	RW	Bit[7:0]: NoiseList3 for L exposure channel RAW de-noise
0x5104	R_NOISELIST4_L_I	0x0C	RW	Bit[7:0]: NoiseList4 for L exposure channel RAW de-noise
0x5105	R_NOISELIST5_L_I	0x10	RW	Bit[7:0]: NoiseList5 for L exposure channel RAW de-noise
0x5106	R_NOISELIST6_L_I	0x12	RW	Bit[7:0]: NoiseList6 for L exposure channel RAW de-noise
0x5107	R_NOISELIST7_L_I	0x18	RW	Bit[7:0]: NoiseList7 for L exposure channel RAW de-noise
0x5108	R_G_DNS_EN_L_I	0x01	RW	Bit[7:1]: Not used Bit[0]: Green channel de-noising for L channel 0: Disable 1: Enable
0x5109	R_NOISE_YSLOP_L_I	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Noise Y slop signal for L channel

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address	register name	default value	R/W	description
0x510A	R_MAX_EDGE_THRE _L_I	0x3F	RW	Bit[7:0]: Maximum edge threshold for L channel
0x510B	R_NOISELIST0_S_I	0x04	RW	Bti[7:0]: NoiseList0 for S exposure channel RAW de-noise
0x510C	R_NOISELIST1_S_I	0x08	RW	Bit[7:0]: NoiseList1 for S exposure channel RAW de-noise
0x510D	R_NOISELIST2_S_I	0x10	RW	Bit[7:0]: NoiseList2 for S exposure channel RAW de-noise
0x510E	R_NOISELIST3_S_I	0x18	RW	Bit[7:0]: NoiseList3 for S exposure channel RAW de-noise
0x510F	R_NOISELIST4_S_I	0x20	RW	Bit[7:0]: NoiseList4 for S exposure channel RAW de-noise
0x5110	R_NOISELIST5_S_I	0x30	RW	Bit[7:0]: NoiseList5 for S exposure channel RAW de-noise
0x5111	R_NOISELIST6_S_I	0x40	RW	Bit[7:0]: NoiseList6 for S exposure channel RAW de-noise
0x5112	R_NOISELIST7_S_I	0x40	RW	Bit[7:0]: NoiseList7 for S exposure channel RAW de-noise
0x5113	R_G_DNS_EN_S_I	0x01	RW	Bit[7:1]: Not used Bit[0]: Green channel de-noising for S channel 0: Disable 1: Enable
0x5114	R_NOISE_YSLOP_S_ I	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Noise Y slop signal S channel
0x5115	R_MAX_EDGE_THRE _S_I	0x3F	RW	Bit[7:0]: Maximum edge threshold S channel
0x5116	R_NOISELIST0_V_I	0x04	RW	Bit[7:0]: NoiseList0 for VS exposure channel RAW de-noise
0x5117	R_NOISELIST1_V_I	0x08	RW	Bit[7:0]: NoiseList1 for VS exposure channel RAW de-noise
0x5118	R_NOISELIST2_V_I	0x10	RW	Bit[7:0]: NoiseList2 for VS exposure channel RAW de-noise
0x5119	R_NOISELIST3_V_I	0x18	RW	Bit[7:0]: NoiseList3 for VS exposure channel RAW de-noise
0x511A	R_NOISELIST4_V_I	0x20	RW	Bit[7:0]: NoiseList4 for VS exposure channel RAW de-noise

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address	register name	default value	R/W	description
0x511B	R_NOISELIST5_V_I	0x30	RW	Bit[7:0]: NoiseList5 for VS exposure channel RAW de-noise
0x511C	R_NOISELIST6_V_I	0x40	RW	Bit[7:0]: NoiseList6 for VS exposure channel RAW de-noise
0x511D	R_NOISELIST7_V_I	0x40	RW	Bit[7:0] NoiseList7 for VS exposure channel RAW de-noise
0x511E	R_G_DNS_EN_V_I	0x00	RW	Bit[7:1]: Not used Bit[0]: Green channel de-noising for VS channel 0: Disable 1: Enable
0x511F	R_NOISE_YSLOP_V_I	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Noise Y slop signal VS channel
0x5120	R_MAX_EDGE_THRE _V_I	0x3F	RW	Bit[7:0]: Maximum edge threshold VS channel
0x5180	R_COMBINE_CTRL	0x0C	RW	Bit[7:4]: Not used Bit[3]: S channel pre matrix enable Bit[2]: Compensate error enable Bit[1:0]: Combine work mode 00: Use combination 01: Use long exposure data as combine result 10: Use short exposure data as combine result 11: Use very short exposure data as combine result
0x5181	R_COMBINE_THRE_0	0x95	RW	Combine Threshold 0 Bit[7:4]: Long Bit[3:0]: Short
0x5182	R_COMBINE_THRE_1	0xA8	RW	Combine Threshold 1 Bit[7:4]: Long Bit[3:0]: Short
0x5183	R_COMBINE_THRE_2	0xAA	RW	Combine Threshold 2 Bit[7:4]: Long Bit[3:0]: Short
0x5184	R_COMBINE_WEIGHT_0 _0	0x80	RW	Bit[7:0]: Combine weight 0,0
0x5185	R_COMBINE_WEIGHT_0 _1	0x80	RW	Bit[7:0]: Combine weight 0,1
0x5186	R_COMBINE_WEIGHT_0 _2	0x60	RW	Bit[7:0]: Combine weight 0,2

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address	register name	default value	R/W	description
0x5187	R_COMBINE_WEIGHT_0_3	0x40	RW	Bit[7:0]: Combine weight 0,3
0x5188	R_COMBINE_WEIGHT_1_0	0x80	RW	Bit[7:0]: Combine weight 1,0
0x5189	R_COMBINE_WEIGHT_1_1	0x80	RW	Bit[7:0]: Combine weight 1,1
0x518A	R_COMBINE_WEIGHT_1_2	0x40	RW	Bit[7:0]: Combine weight 1,2
0x518B	R_COMBINE_WEIGHT_1_3	0x20	RW	Bit[7:0]: Combine weight 1,3
0x518C	R_COMBINE_WEIGHT_2_0	0x80	RW	Bit[7:0]: Combine weight 2,0
0x518D	R_COMBINE_WEIGHT_2_1	0x80	RW	Bit[7:0]: Combine weight 2,1
0X518E	R_COMBINE_WEIGHT_2_2	0x20	RW	Bit[7:0]: Combine weight 2,2
0x518F	R_COMBINE_WEIGHT_2_3	0x00	RW	Bit[7:0]: Combine weight 2,3
0x5190	R_COMBINE_WEIGHT_3_0	0x80	RW	Bit[7:0]: Combine weight 3,0
0x5191	R_COMBINE_WEIGHT_3_1	0x80	RW	Bit[7:0]: Combine weight 3,1
0x5192	R_COMBINE_WEIGHT_3_2	0x00	RW	Bit[7:0]: Combine weight 3,2
0x5193	R_COMBINE_WEIGHT_3_3	0x00	RW	Bit[7:0]: Combine weight 3,3
0x5194	R_SATURATE_THRE_B2	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Final saturate threshold[18:16]
0x5195	R_SATURATE_THRE_B1	0x00	RW	Bit[7:0]: Final saturate threshold[15:8]
0x5196	R_SATURATE_THRE_B0	0x20	RW	Bit[7:0]: Final saturate threshold[7:0]
0x5197	R_TRAFFIC_S_TH_H	0x28	RW	Bit[7:0]: Traffic S threshold[15:8]
0x5198	R_TRAFFIC_S_TH_L	0x00	RW	Bit[7:0]: Traffic S threshold[7:0]
0x5199	R_TH_S_0_H	0x08	RW	Bit[7:0]: m_nThS[0][15:8]
0x519A	R_TH_S_0_L	0x00	RW	Bit[7:0]: m_nThS[0[7:0]

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table A-1 sensor control registers (sheet 33 of 112)

address	register name	default value	R/W	description
0x519B	R_TH_S_1_H	0x10	RW	Bit[7:0]: m_nThS[1][15:8]
0x519C	R_TH_S_1_L	0x00	RW	Bit[7:0]: m_nThS[1][7:0]
0x519D	R_THS_DINV	0x20	RW	Bit[7:0]: m_nThSDinv, equal to (2^16)/(m_nThS[1]-m_nThS[0])
0x51A0~ 0x51F8	RSVD	–	–	Reserved
0x5200	LENC_L_G00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G00 of 8x8 G control point array for L/VS
0x5201	LENC_L_G01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G01 of 8x8 G control point array for L/VS
0x5202	LENC_L_G02	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G02 of 8x8 G control point array for L/VS
0x5203	LENC_L_G03	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G03 of 8x8 G control point array for L/VS
0x5204	LENC_L_G04	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G04 of 8x8 G control point array for L/VS
0x5205	LENC_L_G05	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G05 of 8x8 G control point array for L/VS
0x5206	LENC_L_G06	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G06 of 8x8 G control point array for L/VS
0x5207	LENC_L_G07	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G07 of 8x8 G control point array for L/VS
0x5208	LENC_L_G10	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G10 of 8x8 G control point array for L/VS
0x5209	LENC_L_G11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G11 of 8x8 G control point array for L/VS
0x520A	LENC_L_G12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G12 of 8x8 G control point array for L/VS

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table A-1 sensor control registers (sheet 34 of 112)

address	register name	default value	R/W	description
0x520B	LENC_L_G13	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G13 of 8x8 G control point array for L/VS
0x520C	LENC_L_G14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G14 of 8x8 G control point array for L/VS
0x520D	LENC_L_G15	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G15 of 8x8 G control point array for L/VS
0x520E	LENC_L_G16	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G16 of 8x8 G control point array for L/VS
0x520F	LENC_L_G17	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G17 of 8x8 G control point array for L/VS
0x5210	LENC_L_G20	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G20 of 8x8 G control point array for L/VS
0x5211	LENC_L_G21	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G21 of 8x8 G control point array for L/VS
0x5212	LENC_L_G22	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G22 of 8x8 G control point array for L/VS
0x5213	LENC_L_G23	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G23 of 8x8 G control point array for L/VS
0x5214	LENC_L_G24	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G24 of 8x8 G control point array for L/VS
0x5215	LENC_L_G25	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G25 of 8x8 G control point array for L/VS
0x5216	LENC_L_G26	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G26 of 8x8 G control point array for L/VS
0x5217	LENC_L_G27	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G27 of 8x8 G control point array for L/VS

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table A-1 sensor control registers (sheet 35 of 112)

address	register name	default value	R/W	description
0x5218	LENC_L_G30	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G30 of 8x8 G control point array for L/VS
0x5219	LENC_L_G31	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G31 of 8x8 G control point array for L/VS
0x521A	LENC_L_G32	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G32 of 8x8 G control point array for L/VS
0x521B	LENC_L_G33	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G33 of 8x8 G control point array for L/VS
0x521C	LENC_L_G34	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G34 of 8x8 G control point array for L/VS
0x521D	LENC_L_G35	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G35 of 8x8 G control point array for L/VS
0x521E	LENC_L_G36	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G36 of 8x8 G control point array for L/VS
0x521F	LENC_L_G37	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G37 of 8x8 G control point array for L/VS
0x5220	LENC_L_G40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G40 of 8x8 G control point array for L/VS
0x5221	LENC_L_G41	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G41 of 8x8 G control point array for L/VS
0x5222	LENC_L_G42	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G42 of 8x8 G control point array for L/VS
0x5223	LENC_L_G43	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G43 of 8x8 G control point array for L/VS
0x5224	LENC_L_G44	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G44 of 8x8 G control point array for L/VS

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address	register name	default value	R/W	description
0x5225	LENC_L_G45	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G45 of 8x8 G control point array for L/VS
0x5226	LENC_L_G46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G46 of 8x8 G control point array for L/VS
0x5227	LENC_L_G47	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G47 of 8x8 G control point array for L/VS
0x5228	LENC_L_G50	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G50 of 8x8 G control point array for L/VS
0x5229	LENC_L_G51	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G51 of 8x8 G control point array for L/VS
0x522A	LENC_L_G52	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G52 of 8x8 G control point array for L/VS
0x522B	LENC_L_G53	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G53 of 8x8 G control point array for L/VS
0x522C	LENC_L_G54	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G54 of 8x8 G control point array for L/VS
0x522D	LENC_L_G55	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G55 of 8x8 G control point array for L/VS
0x522E	LENC_L_G56	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G56 of 8x8 G control point array for L/VS
0x522F	LENC_L_G57	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G57 of 8x8 G control point array for L/VS
0x5230	LENC_L_G60	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G60 of 8x8 G control point array for L/VS
0x5231	LENC_L_G61	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G61 of 8x8 G control point array for L/VS

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table A-1 sensor control registers (sheet 37 of 112)

address	register name	default value	R/W	description
0x5232	LENC_L_G62	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G62 of 8x8 G control point array for L/VS
0x5233	LENC_L_G63	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G63 of 8x8 G control point array for L/VS
0x5234	LENC_L_G64	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G64 of 8x8 G control point array for L/VS
0x5235	LENC_L_G65	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G65 of 8x8 G control point array for L/VS
0x5236	LENC_L_G66	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G66 of 8x8 G control point array for L/VS
0x5237	LENC_L_G67	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G67 of 8x8 G control point array for L/VS
0x5238	LENC_L_G70	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G70 of 8x8 G control point array for L/VS
0x5239	LENC_L_G71	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G71 of 8x8 G control point array for L/VS
0x523A	LENC_L_G72	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G72 of 8x8 G control point array for L/VS
0x523B	LENC_L_G73	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G73 of 8x8 G control point array for L/VS
0x523C	LENC_L_G74	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G74 of 8x8 G control point array for L/VS
0x523D	LENC_L_G75	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G75 of 8x8 G control point array for L/VS
0x523E	LENC_L_G76	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G76 of 8x8 G control point array for L/VS

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address	register name	default value	R/W	description
0x523F	LENC_L_G77	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G77 of 8x8 G control point array for L/VS
0x5240	LENC_L_B00	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B00 of 8x8 B control point array for L/VS
0x5241	LENC_L_B01	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B01 of 8x8 B control point array for L/VS
0x5242	LENC_L_B02	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B02 of 8x8 B control point array for L/VS
0x5243	LENC_L_B03	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B03 of 8x8 B control point array for L/VS
0x5244	LENC_L_B04	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B04 of 8x8 B control point array for L/VS
0x5245	LENC_L_B05	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B05 of 8x8 B control point array for L/VS
0x5246	LENC_L_B06	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B06 of 8x8 B control point array for L/VS
0x5247	LENC_L_B07	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B07 of 8x8 B control point array for L/VS
0x5248	LENC_L_B10	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B10 of 8x8 B control point array for L/VS
0x5249	LENC_L_B11	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B11 of 8x8 B control point array for L/VS
0x524A	LENC_L_B12	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B12 of 8x8 B control point array for L/VS
0x524B	LENC_L_B13	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B13 of 8x8 B control point array for L/VS

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table A-1 sensor control registers (sheet 39 of 112)

address	register name	default value	R/W	description
0x524C	LENC_L_B14	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B14 of 8x8 B control point array for L/VS
0x524D	LENC_L_B15	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B15 of 8x8 B control point array for L/VS
0x524E	LENC_L_B16	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B16 of 8x8 B control point array for L/VS
0x524F	LENC_L_B17	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B17 of 8x8 B control point array for L/VS
0x5250	LENC_L_B20	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B20 of 8x8 B control point array for L/VS
0x5251	LENC_L_B21	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B21 of 8x8 B control point array for L/VS
0x5252	LENC_L_B22	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B22 of 8x8 B control point array for L/VS
0x5253	LENC_L_B23	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B23 of 8x8 B control point array for L/VS
0x5254	LENC_L_B24	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B24 of 8x8 B control point array for L/VS
0x5255	LENC_L_B25	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B25 of 8x8 B control point array for L/VS
0x5256	LENC_L_B26	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B26 of 8x8 B control point array for L/VS
0x5257	LENC_L_B27	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B27 of 8x8 B control point array for L/VS
0x5258	LENC_L_B30	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B30 of 8x8 B control point array for L/VS

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table A-1 sensor control registers (sheet 40 of 112)

address	register name	default value	R/W	description
0x5259	LENC_L_B31	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B31 of 8x8 B control point array for L/VS
0x525A	LENC_L_B32	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B32 of 8x8 B control point array for L/VS
0x525B	LENC_L_B33	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B33 of 8x8 B control point array for L/VS
0x525C	LENC_L_B34	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B34 of 8x8 B control point array for L/VS
0x525D	LENC_L_B35	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B35 of 8x8 B control point array for L/VS
0x525E	LENC_L_B36	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B36 of 8x8 B control point array for L/VS
0x525F	LENC_L_B37	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B37 of 8x8 B control point array for L/VS
0x5260	LENC_L_B40	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B40 of 8x8 B control point array for L/VS
0x5261	LENC_L_B41	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B41 of 8x8 B control point array for L/VS
0x5262	LENC_L_B42	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B42 of 8x8 B control point array for L/VS
0x5263	LENC_L_B43	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B43 of 8x8 B control point array for L/VS
0x5264	LENC_L_B44	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B44 of 8x8 B control point array for L/VS
0x5265	LENC_L_B45	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B45 of 8x8 B control point array for L/VS

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table A-1 sensor control registers (sheet 41 of 112)

address	register name	default value	R/W	description
0x5266	LENC_L_B46	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B46 of 8x8 B control point array for L/VS
0x5267	LENC_L_B47	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B47 of 8x8 B control point array for L/VS
0x5268	LENC_L_B50	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B50 of 8x8 B control point array for L/VS
0x5269	LENC_L_B51	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B51 of 8x8 B control point array for L/VS
0x526A	LENC_L_B52	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B52 of 8x8 B control point array for L/VS
0x526B	LENC_L_B53	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B53 of 8x8 B control point array for L/VS
0x526C	LENC_L_B54	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B54 of 8x8 B control point array for L/VS
0x526D	LENC_L_B55	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B55 of 8x8 B control point array for L/VS
0x526E	LENC_L_B56	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B56 of 8x8 B control point array for L/VS
0x526F	LENC_L_B57	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B57 of 8x8 B control point array for L/VS
0x5270	LENC_L_B60	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B60 of 8x8 B control point array for L/VS
0x5271	LENC_L_B61	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B61 of 8x8 B control point array for L/VS
0x5272	LENC_L_B62	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B62 of 8x8 B control point array for L/VS

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table A-1 sensor control registers (sheet 42 of 112)

address	register name	default value	R/W	description
0x5273	LENC_L_B63	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B63 of 8x8 B control point array for L/VS
0x5274	LENC_L_B64	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B64 of 8x8 B control point array for L/VS
0x5275	LENC_L_B65	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B65 of 8x8 B control point array for L/VS
0x5276	LENC_L_B66	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B66 of 8x8 B control point array for L/VS
0x5277	LENC_L_B67	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B67 of 8x8 B control point array for L/VS
0x5278	LENC_L_B70	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B70 of 8x8 B control point array for L/VS
0x5279	LENC_L_B71	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B71 of 8x8 B control point array for L/VS
0x527A	LENC_L_B72	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B72 of 8x8 B control point array for L/VS
0x527B	LENC_L_B73	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B73 of 8x8 B control point array for L/VS
0x527C	LENC_L_B74	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B74 of 8x8 B control point array for L/VS
0x527D	LENC_L_B75	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B75 of 8x8 B control point array for L/VS
0x527E	LENC_L_B76	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B76 of 8x8 B control point array for L/VS
0x527F	LENC_L_B77	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B77 of 8x8 B control point array for L/VS

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table A-1 sensor control registers (sheet 43 of 112)

address	register name	default value	R/W	description
0x5280	LENC_L_R00	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R00 of 8x8 R control point array for L/VS
0x5281	LENC_L_R01	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R01 of 8x8 R control point array for L/VS
0x5282	LENC_L_R02	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R02 of 8x8 R control point array for L/VS
0x5283	LENC_L_R03	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R03 of 8x8 R control point array for L/VS
0x5284	LENC_L_R04	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R04 of 8x8 R control point array for L/VS
0x5285	LENC_L_R05	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R05 of 8x8 R control point array for L/VS
0x5286	LENC_L_R06	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R06 of 8x8 R control point array for L/VS
0x5287	LENC_L_R07	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R07 of 8x8 R control point array for L/VS
0x5288	LENC_L_R10	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R10 of 8x8 R control point array for L/VS
0x5289	LENC_L_R11	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R11 of 8x8 R control point array for L/VS
0x528A	LENC_L_R12	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R12 of 8x8 R control point array for L/VS
0x528B	LENC_L_R13	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R13 of 8x8 R control point array for L/VS
0x528C	LENC_L_R14	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R14 of 8x8 R control point array for L/VS

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table A-1 sensor control registers (sheet 44 of 112)

address	register name	default value	R/W	description
0x528D	LENC_L_R15	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R15 of 8x8 R control point array for L/VS
0x528E	LENC_L_R16	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R16 of 8x8 R control point array for L/VS
0x528F	LENC_L_R17	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R17 of 8x8 R control point array for L/VS
0x5290	LENC_L_R20	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R20 of 8x8 R control point array for L/VS
0x5291	LENC_L_R21	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R21 of 8x8 R control point array for L/VS
0x5292	LENC_L_R22	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R22 of 8x8 R control point array for L/VS
0x5293	LENC_L_R23	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R23 of 8x8 R control point array for L/VS
0x5294	LENC_L_R24	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R24 of 8x8 R control point array for L/VS
0x5295	LENC_L_R25	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R25 of 8x8 R control point array for L/VS
0x5296	LENC_L_R26	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R26 of 8x8 R control point array for L/VS
0x5297	LENC_L_R27	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R27 of 8x8 R control point array for L/VS
0x5298	LENC_L_R30	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R30 of 8x8 R control point array for L/VS
0x5299	LENC_L_R31	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R31 of 8x8 R control point array for L/VS

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table A-1 sensor control registers (sheet 45 of 112)

address	register name	default value	R/W	description
0x529A	LENC_L_R32	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R32 of 8x8 R control point array for L/VS
0x529B	LENC_L_R33	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R33 of 8x8 R control point array for L/VS
0x529C	LENC_L_R34	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R34 of 8x8 R control point array for L/VS
0x529D	LENC_L_R35	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R35 of 8x8 R control point array for L/VS
0x529E	LENC_L_R36	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R36 of 8x8 R control point array for L/VS
0x529F	LENC_L_R37	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R37 of 8x8 R control point array for L/VS
0x52A0	LENC_L_R40	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R40 of 8x8 R control point array for L/VS
0x52A1	LENC_L_R41	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R41 of 8x8 R control point array for L/VS
0x52A2	LENC_L_R42	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R42 of 8x8 R control point array for L/VS
0x52A3	LENC_L_R43	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R43 of 8x8 R control point array for L/VS
0x52A4	LENC_L_R44	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R44 of 8x8 R control point array for L/VS
0x52A5	LENC_L_R45	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R45 of 8x8 R control point array for L/VS
0x52A6	LENC_L_R46	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R46 of 8x8 R control point array for L/VS

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table A-1 sensor control registers (sheet 46 of 112)

address	register name	default value	R/W	description
0x52A7	LENC_L_R47	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R47 of 8x8 R control point array for L/VS
0x52A8	LENC_L_R50	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R50 of 8x8 R control point array for L/VS
0x52A9	LENC_L_R51	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R51 of 8x8 R control point array for L/VS
0x52AA	LENC_L_R52	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R52 of 8x8 R control point array for L/VS
0x52AB	LENC_L_R53	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R53 of 8x8 R control point array for L/VS
0x52AC	LENC_L_R54	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R54 of 8x8 R control point array for L/VS
0x52AD	LENC_L_R55	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R55 of 8x8 R control point array for L/VS
0x52AE	LENC_L_R56	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R56 of 8x8 R control point array for L/VS
0x52AF	LENC_L_R57	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R57 of 8x8 R control point array for L/VS
0x52B0	LENC_L_R60	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R60 of 8x8 R control point array for L/VS
0x52B1	LENC_L_R61	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R61 of 8x8 R control point array for L/VS
0x52B2	LENC_L_R62	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R62 of 8x8 R control point array for L/VS
0x52B3	LENC_L_R63	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R63 of 8x8 R control point array for L/VS

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table A-1 sensor control registers (sheet 47 of 112)

address	register name	default value	R/W	description
0x52B4	LENC_L_R64	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R64 of 8x8 R control point array for L/VS
0x52B5	LENC_L_R65	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R65 of 8x8 R control point array for L/VS
0x52B6	LENC_L_R66	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R66 of 8x8 R control point array for L/VS
0x52B7	LENC_L_R67	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R67 of 8x8 R control point array for L/VS
0x52B8	LENC_L_R70	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R70 of 8x8 R control point array for L/VS
0x52B9	LENC_L_R71	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R71 of 8x8 R control point array for L/VS
0x52BA	LENC_L_R72	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R72 of 8x8 R control point array for L/VS
0x52BB	LENC_L_R73	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R73 of 8x8 R control point array for L/VS
0x52BC	LENC_L_R74	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R74 of 8x8 R control point array for L/VS
0x52BD	LENC_L_R75	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R75 of 8x8 R control point array for L/VS
0x52BE	LENC_L_R76	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R76 of 8x8 R control point array for L/VS
0x52BF	LENC_L_R77	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R77 of 8x8 R control point array for L/VS
0x52C0	LENC_S_G00	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G00 of 8x8 G control point array for S

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table A-1 sensor control registers (sheet 48 of 112)

address	register name	default value	R/W	description
0x52C1	LENC_S_G01	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G01 of 8x8 G control point array for S
0x52C2	LENC_S_G02	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G02 of 8x8 G control point array for S
0x52C3	LENC_S_G03	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G03 of 8x8 G control point array for S
0x52C4	LENC_S_G04	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G04 of 8x8 G control point array for S
0x52C5	LENC_S_G05	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G05 of 8x8 G control point array for S
0x52C6	LENC_S_G06	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G06 of 8x8 G control point array for S
0x52C7	LENC_S_G07	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G07 of 8x8 G control point array for S
0x52C8	LENC_S_G10	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G10 of 8x8 G control point array for S
0x52C9	LENC_S_G11	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G11 of 8x8 G control point array for S
0x52CA	LENC_S_G12	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G12 of 8x8 G control point array for S
0x52CB	LENC_S_G13	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G13 of 8x8 G control point array for S
0x52CC	LENC_S_G14	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G14 of 8x8 G control point array for S
0x52CD	LENC_S_G15	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G15 of 8x8 G control point array for S
0x52CE	LENC_S_G16	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G16 of 8x8 G control point array for S

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table A-1 sensor control registers (sheet 49 of 112)

address	register name	default value	R/W	description
0x52CF	LENC_S_G17	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G17 of 8x8 G control point array for S
0x52D0	LENC_S_G20	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G20 of 8x8 G control point array for S
0x52D1	LENC_S_G21	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G21 of 8x8 G control point array for S
0x52D2	LENC_S_G22	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G22 of 8x8 G control point array for S
0x52D3	LENC_S_G23	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G23 of 8x8 G control point array for S
0x52D4	LENC_S_G24	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G24 of 8x8 G control point array for S
0x52D5	LENC_S_G25	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G25 of 8x8 G control point array for S
0x52D6	LENC_S_G26	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G26 of 8x8 G control point array for S
0x52D7	LENC_S_G27	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G27 of 8x8 G control point array for S
0x52D8	LENC_S_G30	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G30 of 8x8 G control point array for S
0x52D9	LENC_S_G31	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G31 of 8x8 G control point array for S
0x52DA	LENC_S_G32	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G32 of 8x8 G control point array for S
0x52DB	LENC_S_G33	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G33 of 8x8 G control point array for S

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table A-1 sensor control registers (sheet 50 of 112)

address	register name	default value	R/W	description
0x52DC	LENC_S_G34	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G34 of 8x8 G control point array for S
0x52DD	LENC_S_G35	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G35 of 8x8 G control point array for S
0x52DE	LENC_S_G36	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G36 of 8x8 G control point array for S
0x52DF	LENC_S_G37	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G37 of 8x8 G control point array for S
0x52E0	LENC_S_G40	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G40 of 8x8 G control point array for S
0x52E1	LENC_S_G41	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G41 of 8x8 G control point array for S
0x52E2	LENC_S_G42	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G42 of 8x8 G control point array for S
0x52E3	LENC_S_G43	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G43 of 8x8 G control point array for S
0x52E4	LENC_S_G44	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G44 of 8x8 G control point array for S
0x52E5	LENC_S_G45	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G45 of 8x8 G control point array for S
0x52E6	LENC_S_G46	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G46 of 8x8 G control point array for S
0x52E7	LENC_S_G47	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G47 of 8x8 G control point array for S
0x52E8	LENC_S_G50	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G50 of 8x8 G control point array for S

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table A-1 sensor control registers (sheet 51 of 112)

address	register name	default value	R/W	description
0x52E9	LENC_S_G51	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G51 of 8x8 G control point array for S
0x52EA	LENC_S_G52	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G52 of 8x8 G control point array for S
0x52EB	LENC_S_G53	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G53 of 8x8 G control point array for S
0x52EC	LENC_S_G54	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G54 of 8x8 G control point array for S
0x52ED	LENC_S_G55	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G55 of 8x8 G control point array for S
0x52EE	LENC_S_G56	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G56 of 8x8 G control point array for S
0x52EF	LENC_S_G57	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G57 of 8x8 G control point array for S
0x52F0	LENC_S_G60	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G60 of 8x8 G control point array for S
0x52F1	LENC_S_G61	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G61 of 8x8 G control point array for S
0x52F2	LENC_S_G62	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G62 of 8x8 G control point array for S
0x52F3	LENC_S_G63	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G63 of 8x8 G control point array for S
0x52F4	LENC_S_G64	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G64 of 8x8 G control point array for S
0x52F5	LENC_S_G65	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G65 of 8x8 G control point array for S

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table A-1 sensor control registers (sheet 52 of 112)

address	register name	default value	R/W	description
0x52F6	LENC_S_G66	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G66 of 8x8 G control point array for S
0x52F7	LENC_S_G67	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G67 of 8x8 G control point array for S
0x52F8	LENC_S_G70	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G70 of 8x8 G control point array for S
0x52F9	LENC_S_G71	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G71 of 8x8 G control point array for S
0x52FA	LENC_S_G72	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G72 of 8x8 G control point array for S
0x52FB	LENC_S_G73	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G73 of 8x8 G control point array for S
0x52FC	LENC_S_G74	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G74 of 8x8 G control point array for S
0x52FD	LENC_S_G75	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G75 of 8x8 G control point array for S
0x52FE	LENC_S_G76	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G76 of 8x8 G control point array for S
0x52FF	LENC_S_G77	0x00	RW	Bit[7:6]: Not used Bit[5:0]: G77 of 8x8 G control point array for S
0x5300	LENC_S_B00	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B00 of 8x8 B control point array for S
0x5301	LENC_S_B01	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B01 of 8x8 B control point array for S
0x5302	LENC_S_B02	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B02 of 8x8 B control point array for S
0x5303	LENC_S_B03	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B03 of 8x8 B control point array for S
0x5304	LENC_S_B04	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B04 of 8x8 B control point array for S

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address	register name	default value	R/W	description
0x5305	LENC_S_B05	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B05 of 8x8 B control point array for S
0x5306	LENC_S_B06	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B06 of 8x8 B control point array for S
0x5307	LENC_S_B07	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B07 of 8x8 B control point array for S
0x5308	LENC_S_B10	0x20	RW	Bit[7:6]: Not used Bti[5:0]: B10 of 8x8 B control point array for S
0x5309	LENC_S_B11	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B11 of 8x8 B control point array for S
0x530A	LENC_S_B12	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B12 of 8x8 B control point array for S
0x530B	LENC_S_B13	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B13 of 8x8 B control point array for S
0x530C	LENC_S_B14	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B14 of 8x8 B control point array for S
0x530D	LENC_S_B15	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B15 of 8x8 B control point array for S
0x530E	LENC_S_B16	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B16 of 8x8 B control point array for S
0x530F	LENC_S_B17	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B17 of 8x8 B control point array for S
0x5310	LENC_S_B20	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B20 of 8x8 B control point array for S
0x5311	LENC_S_B21	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B21 of 8x8 B control point array for S
0x5312	LENC_S_B22	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B22 of 8x8 B control point array for S
0x5313	LENC_S_B23	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B23 of 8x8 B control point array for S
0x5314	LENC_S_B24	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B24 of 8x8 B control point array for S
0x5315	LENC_S_B25	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B25 of 8x8 B control point array for S
0x5316	LENC_S_B26	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B26 of 8x8 B control point array for S
0x5317	LENC_S_B27	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B27 of 8x8 B control point array for S

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table A-1 sensor control registers (sheet 54 of 112)

address	register name	default value	R/W	description
0x5318	LENC_S_B30	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B30 of 8x8 B control point array for S
0x5319	LENC_S_B31	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B31 of 8x8 B control point array for S
0x531A	LENC_S_B32	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B32 of 8x8 B control point array for S
0x531B	LENC_S_B33	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B33 of 8x8 B control point array for S
0x531C	LENC_S_B34	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B34 of 8x8 B control point array for S
0x531D	LENC_S_B35	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B35 of 8x8 B control point array for S
0x531E	LENC_S_B36	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B36 of 8x8 B control point array for S
0x531F	LENC_S_B37	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B37 of 8x8 B control point array for S
0x5320	LENC_S_B40	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B40 of 8x8 B control point array for S
0x5321	LENC_S_B41	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B41 of 8x8 B control point array for S
0x5322	LENC_S_B42	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B42 of 8x8 B control point array for S
0x5323	LENC_S_B43	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B43 of 8x8 B control point array for S
0x5324	LENC_S_B44	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B44 of 8x8 B control point array for S
0x5325	LENC_S_B45	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B45 of 8x8 B control point array for S
0x5326	LENC_S_B46	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B46 of 8x8 B control point array for S
0x5327	LENC_S_B47	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B47 of 8x8 B control point array for S
0x5328	LENC_S_B50	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B50 of 8x8 B control point array for S
0x5329	LENC_S_B51	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B51 of 8x8 B control point array for S
0x532A	LENC_S_B52	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B52 of 8x8 B control point array for S

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address	register name	default value	R/W	description
0x532B	LENC_S_B53	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B53 of 8x8 B control point array for S
0x532C	LENC_S_B54	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B54 of 8x8 B control point array for S
0x532D	LENC_S_B55	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B55 of 8x8 B control point array for S
0x532E	LENC_S_B56	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B56 of 8x8 B control point array for S
0x532F	LENC_S_B57	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B57 of 8x8 B control point array for S
0x5330	LENC_S_B60	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B60 of 8x8 B control point array for S
0x5331	LENC_S_B61	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B61 of 8x8 B control point array for S
0x5332	LENC_S_B62	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B62 of 8x8 B control point array for S
0x5333	LENC_S_B63	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B63 of 8x8 B control point array for S
0x5334	LENC_S_B64	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B64 of 8x8 B control point array for S
0x5335	LENC_S_B65	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B65 of 8x8 B control point array for S
0x5336	LENC_S_B66	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B66 of 8x8 B control point array for S
0x5337	LENC_S_B67	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B67 of 8x8 B control point array for S
0x5338	LENC_S_B70	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B70 of 8x8 B control point array for S
0x5339	LENC_S_B71	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B71 of 8x8 B control point array for S
0x533A	LENC_S_B72	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B72 of 8x8 B control point array for S
0x533B	LENC_S_B73	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B73 of 8x8 B control point array for S
0x533C	LENC_S_B74	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B74 of 8x8 B control point array for S
0x533D	LENC_S_B75	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B75 of 8x8 B control point array for S

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table A-1 sensor control registers (sheet 56 of 112)

address	register name	default value	R/W	description
0x533E	LENC_S_B76	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B76 of 8x8 B control point array for S
0x533F	LENC_S_B77	0x20	RW	Bit[7:6]: Not used Bit[5:0]: B77 of 8x8 B control point array for S
0x5340	LENC_S_R00	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R00 of 8x8 R control point array for S
0x5341	LENC_S_R01	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R01 of 8x8 R control point array for S
0x5342	LENC_S_R02	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R02 of 8x8 R control point array for S
0x5343	LENC_S_R03	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R03 of 8x8 R control point array for S
0x5344	LENC_S_R04	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R04 of 8x8 R control point array for S
0x5345	LENC_S_R05	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R05 of 8x8 R control point array for S
0x5346	LENC_S_R06	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R06 of 8x8 R control point array for S
0x5347	LENC_S_R07	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R07 of 8x8 R control point array for S
0x5348	LENC_S_R10	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R10 of 8x8 R control point array for S
0x5349	LENC_S_R11	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R11 of 8x8 R control point array for S
0x534A	LENC_S_R12	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R12 of 8x8 R control point array for S
0x534B	LENC_S_R13	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R13 of 8x8 R control point array for S
0x534C	LENC_S_R14	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R14 of 8x8 R control point array for S
0x534D	LENC_S_R15	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R15 of 8x8 R control point array for S
0x534E	LENC_S_R16	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R16 of 8x8 R control point array for S
0x534F	LENC_S_R17	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R17 of 8x8 R control point array for S
0x5350	LENC_S_R20	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R20 of 8x8 R control point array for S

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address	register name	default value	R/W	description
0x5351	LENC_S_R21	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R21 of 8x8 R control point array for S
0x5352	LENC_S_R22	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R22 of 8x8 R control point array for S
0x5353	LENC_S_R23	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R23 of 8x8 R control point array for S
0x5354	LENC_S_R24	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R24 of 8x8 R control point array for S
0x5355	LENC_S_R25	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R25 of 8x8 R control point array for S
0x5356	LENC_S_R26	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R26 of 8x8 R control point array for S
0x5357	LENC_S_R27	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R27 of 8x8 R control point array for S
0x5358	LENC_S_R30	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R30 of 8x8 R control point array for S
0x5359	LENC_S_R31	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R31 of 8x8 R control point array for S
0x535A	LENC_S_R32	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R32 of 8x8 R control point array for S
0x535B	LENC_S_R33	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R33 of 8x8 R control point array for S
0x535C	LENC_S_R34	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R34 of 8x8 R control point array for S
0x535D	LENC_S_R35	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R35 of 8x8 R control point array for S
0x535E	LENC_S_R36	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R36 of 8x8 R control point array for S
0x535F	LENC_S_R37	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R37 of 8x8 R control point array for S
0x5360	LENC_S_R40	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R40 of 8x8 R control point array for S
0x5361	LENC_S_R41	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R41 of 8x8 R control point array for S
0x5362	LENC_S_R42	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R42 of 8x8 R control point array for S
0x5363	LENC_S_R43	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R43 of 8x8 R control point array for S

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table A-1 sensor control registers (sheet 58 of 112)

address	register name	default value	R/W	description
0x5364	LENC_S_R44	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R44 of 8x8 R control point array for S
0x5365	LENC_S_R45	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R45 of 8x8 R control point array for S
0x5366	LENC_S_R46	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R46 of 8x8 R control point array for S
0x5367	LENC_S_R47	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R47 of 8x8 R control point array for S
0x5368	LENC_S_R50	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R50 of 8x8 R control point array for S
0x5369	LENC_S_R51	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R51 of 8x8 R control point array for S
0x536A	LENC_S_R52	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R52 of 8x8 R control point array for S
0x536B	LENC_S_R53	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R53 of 8x8 R control point array for S
0x536C	LENC_S_R54	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R54 of 8x8 R control point array for S
0x536D	LENC_S_R55	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R55 of 8x8 R control point array for S
0x536E	LENC_S_R56	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R56 of 8x8 R control point array for S
0x536F	LENC_S_R57	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R57 of 8x8 R control point array for S
0x5370	LENC_S_R60	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R60 of 8x8 R control point array for S
0x5371	LENC_S_R61	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R61 of 8x8 R control point array for S
0x5372	LENC_S_R62	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R62 of 8x8 R control point array for S
0x5373	LENC_S_R63	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R63 of 8x8 R control point array for S
0x5374	LENC_S_R64	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R64 of 8x8 R control point array for S
0x5375	LENC_S_R65	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R65 of 8x8 R control point array for S
0x5376	LENC_S_R66	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R66 of 8x8 R control point array for S

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table A-1 sensor control registers (sheet 59 of 112)

address	register name	default value	R/W	description
0x5377	LENC_S_R67	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R67 of 8x8 R control point array for S
0x5378	LENC_S_R70	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R70 of 8x8 R control point array for S
0x5379	LENC_S_R71	0x20	RW	Bit[7:6]: Not used Bit[5:0] R71 of 8x8 R control point array for S
0x537A	LENC_S_R72	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R72 of 8x8 R control point array for S
0x537B	LENC_S_R73	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R73 of 8x8 R control point array for S
0x537C	LENC_S_R74	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R74 of 8x8 R control point array for S
0x537D	LENC_S_R75	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R75 of 8x8 R control point array for S
0x537E	LENC_S_R76	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R76 of 8x8 R control point array for S
0x537F	LENC_S_R77	0x20	RW	Bit[7:6]: Not used Bit[5:0]: R77 of 8x8 R control point array for S
0x5380	LENC_CTRL10	0x0D	RW	Bit[7:4]: Not used Bit[3]: m_nq_option L/S/VS employ same m_nq of L Bit[2]: Gain 0: Do not allow less than 1x gain 1: Allow less than 1x gain to apply to pixel Bit[1]: rand_bit_en_l (active high) Add random enable for L/VS Bit[0]: Luminance 0: Luminance compensation amplitude does not change with sensor gain 1: Luminance compensation amplitude changes with camera gain
0x5381	MAXGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Maxgain[11:8] If 0x5380[0]=1 and sensor gain is bigger than this threshold, luminance compensation amplitude will be minimum value (0x5385)

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table A-1 sensor control registers (sheet 60 of 112)

address	register name	default value	R/W	description
0x5382	MAXGAIN_L_BYTE0	0x60	RW	Bit[7:0]: Maxgain[7:0] If 0x5380[0]=1 and sensor gain is bigger than this threshold, luminance compensation amplitude will be minimum value (0x5385)
0x5383	MINGAIN_L_BYTE1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Mingain[11:8] If 0x5380[0]=1 and sensor gain is smaller than this threshold, luminance compensation amplitude will be maximum value (0x5386)
0x5384	MINGAIN_L_BYTE0	0x20	RW	Bit[7:0]: Mingain[7:0] If 0x5380[0]=1 and sensor gain is smaller than this threshold, luminance compensation amplitude will be maximum value (0x5386)
0x5385	MINQ_L	0x18	RW	Bit[7]: Not used Bit[6:0]: Value indicates minimum amplitude which luminance channel compensates when 0x5380[0]=1
0x5386	MAXQ_L	0x40	RW	Bit[7]: Not used Bit[6:0]: Value indicates maximum amplitude which luminance channel compensates when 0x5380[0]=1
0x5387	BR_HSCALE_L_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: BR_HSCALE[10:8] For horizontal color gain calculation, this value indicates step between two connected horizontal pixels
0x5388	BR_HSCALE_L_BYTE0	0x0A	RW	Bit[7:0]: BR_HSCALE[7:0] For horizontal color gain calculation, this value indicates step between two connected horizontal pixels
0x5389	BR_VSCALE_L_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: BR_VSCALE[10:8] For vertical color gain calculation, value indicates step between two connected vertical pixels
0x538A	BR_VSCALE_L_BYTE0	0xF4	RW	Bit[7:0]: BR_VSCALE[7:0] For vertical color gain calculation, value indicates step between two connected vertical pixels

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address	register name	default value	R/W	description
0x538B	G_HSCALE_L_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: G_HSCALE[10:8] For horizontal luminance gain calculation, this value indicates step between two connected horizontal pixels
0x538C	G_HSCALE_L_BYTE0	0x06	RW	Bit[7:0]: G_HSCALE[7:0] For horizontal luminance gain calculation, this value indicates step between two connected horizontal pixels
0x538D	G_VSCALE_L_BYTE1	0x01	RW	Bit[7:3]: Not used Bit[2:0]: G_VSCALE[10:8] For vertical luminance gain calculation, value indicates step between two connection vertical pixels
0x538E	G_VSCALE_L_BYTE0	0x6A	RW	Bit[7:0]: G_VSCALE[7:0] For vertical luminance gain calculation, value indicates step between two connection vertical pixels
0x538F	LENC_CTRL11	0x6A	RW	Bit[7:3]: Not used Bit[2]: less_1x_en_s (active high) Less than 1x gain enable for S Bit[1]: rand_bit_en_s (active high) Add random enable for S Bit[0]: auto_q_en_s (active high) Auto calculation Q enable for S
0x5390	MAXGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Upper gain threshold for auto Q, for S[11:8]
0x5391	MAXGAIN_S_BYTE0	0x60	RW	Bit[7:0]: Upper gain threshold for auto Q, for S[7:0]
0x5392	MINGAIN_S_BYTE1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Lower gain threshold for auto Q, for S[11:8]
0x5393	MINGAIN_S_BYTE0	0x20	RW	Bit[7:0]: Lower gain threshold for auto Q, for S[7:0]
0x5394	MINQ_S	0x18	RW	Bit[7]: Not used Bit[6:0]: Minimum Q for auto Q when gain larger than maxgain, for S

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address	register name	default value	R/W	description
0x5395	MAXQ_S	0x40	RW	Bit[7]: Not used Bit[6:0]: Maximum Q for auto Q when gain smaller than mingain, for S
0x5396	BR_HSCALE_S_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: H scale for blue/red channel for S[10:8]
0x5397	BR_HSCALE_S_BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for S[7:0]
0x5398	BR_VSCALE_S_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: V scale for blue/red channel for S[10:8]
0x5399	BR_VSCALE_S_BYTE0	0xF4	RW	Bit[7:0]: V scale for blue/red channel for S[7:0]
0x539A	G_HSCALE_S_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: H scale for blue/red channel for S[10:8]
0x539B	G_HSCALE_S_BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for S[7:0]
0x539C	G_VSCALE_S_BYTE1	0x01	RW	Bit[7:3]: Not used Bit[2:0]: V scale for blue/red channel for S[10:8]
0x539D	G_VSCALE_S_BYTE0	0x7A	RW	Bit[7:0]: V scale for blue/red channel for S[7:0]
0x539E	BR_HSCALE_VS _BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: H scale for blue/red channel for VS[10:8]
0x539F	BR_HSCALE_VS _BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for VS[7:0]
0x53A0	BR_VSCALE_VS _BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: V scale for blue/red channel for VS[10:8]
0x53A1	BR_VSCALE_VS _BYTE0	0xF4	RW	Bit[7:0]: V scale for blue/red channel for VS[7:0]
0x53A2	G_HSCALE_VS_BYTE1	0x02	RW	Bit[7:3]: Not used Bit[2:0]: H scale for blue/red channel for VS[10:8]
0x53A3	G_HSCALE_VS_BYTE0	0x0A	RW	Bit[7:0]: H scale for blue/red channel for VS[7:0]

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address	register name	default value	R/W	description
0x53A4	G_VSCALE_VS_BYTE1	0x01	RW	Bit[7:3]: Not used Bit[2:0]: V scale for blue/red channel for VS[10:8]
0x53A5	G_VSCALE_VS_BYTE0	0x7A	RW	Bit[7:0]: V scale for blue/red channel for VS[7:0]
0x53A6~ 0x53A8	RSVD	–	–	Reserved
0x53A9	M_NQ_L	–	R	Bit[7]: Not used Bit[6:0]: m_nQ effective for L
0x53AA	M_NQ_S	–	R	Bit[7]: Not used Bit[6:0]: m_nQ effective for S
0x53AB	M_NQ_VS	–	R	Bit[7]: Not used Bit[6:0]: m_nQ effective for VS
0x5400~ 0x5523	FW_HDR	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.
0x5524~ 0x553F	RSVD	–	–	Reserved
0x550C	HT_ISP	0x09	RW	Bit[7:4]: Not used Bit[3]: Dark current and gain based BLC compensation Bit[2]: New night mode enable Bit[1:0]: Reserved

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address	register name	default value	R/W	description
0x5580	TONE_MAPPING_CTRL0	0x03	RW	Bit[7:5]: global_mean_sh ROI statistic pixel selection 000: All pixels in ROI are used for statistics 001: 1/4 sample in both horizontal and vertical direction 010: 1/16 sample in both horizontal and vertical direction 011: 1/64 sample in both horizontal and vertical direction 100: 1/256 sample in both horizontal and vertical direction Others: Not supported Bit[4]: global_mean_roi_en 0: Global mean is calculated from local mean by getting average value of 4x4 window local mean 1: Global mean is calculated from selected ROI Bit[3]: hdr_gain_sh_en 0: Use log value directly from combine output 1: Add a shift value to compensate combine output log value Bit[2]: Enable fish eye statistics 0: All pixels in corner windows are effective 1: For pixels in four corner windows, only inner triangle pixels are effective Bit[1]: Contrast boost enable Bit[0]: Contrast enable
0x5581~ 0x5589	RSVD	–	–	Reserved
0x558A	TONE_MAPPING_CTRL2	0x0A	RW	Bit[7:6]: Not used Bit[5]: Enable manual output bit-width 0: Use auto raw_out_bit value from input port 1: Use manual raw_out_bit value from internal register Bit[4:0]: raw_out_bit
0x558B	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x558C	ROI_TOP_BYTE1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI top boundary line[9:8]
0x558D	ROI_TOP_BYTE0	0x10	RW	Bit[7:0]: ROI top boundary line[7:0]
0x558E	ROI_BOTTOM_BYTE1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI bottom boundary line[9:8]
0x558F	ROI_BOTTOM_BYTE0	0x10	RW	Bit[7:0]: ROI bottom boundary line[7:0]
0x5590	ROI_LEFT_BYTE1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI left boundary column[9:8]
0x5591	ROI_LEFT_BYTE0	0x10	RW	Bit[7:0]: ROI left boundary column[7:0]
0x5592	ROI_RIGHT_BYTE1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI right boundary column[9:8]
0x5593	ROI_RIGHT_BYTE0	0x10	RW	Bit[7:0]: ROI right boundary column[7:0]
0x5594	GLOBAL_ST_TH_ BYTE2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Global mean statistic threshold[19:16]
0x5595	GLOBAL_ST_TH_ BYTE1	0x04	RW	Bit[7:0]: Global mean statistic threshold[15:8]
0x5596	GLOBAL_ST_TH_ BYTE0	0x00	RW	Bit[7:0]: Global mean statistic threshold[7:0]
0x5597	HDR_GAIN_SH_BYTE1	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Log HDR gain shift[12:8]
0x5598	HDR_GAIN_SH_BYTE0	0x00	RW	Bit[7:0]: Log HDR gain shift[7:0]
0x5599~ 0x5617	RSVD	–	–	Reserved
0x5618	Y_TH0_BYTE1	0x00	RW	Bit[7:0]: Y threshold 0[15:8]
0x5619	Y_TH0_BYTE0	0x00	RW	Bit[7:0]: Y threshold 0[7:0]
0x561A	Y_TH1_BYTE1	0x00	RW	Bit[7:0]: Y threshold 1[15:8]
0x561B	Y_TH1_BYTE0	0x00	RW	Bit[7:0]: Y threshold 1[7:0]
0x561C	Y_TH2_BYTE1	0x00	RW	Bit[7:0]: Y threshold 2[15:8]
0x561D	Y_TH2_BYTE0	0x00	RW	Bit[7:0]: Y threshold 2[7:0]
0x561E	Y_TH3_BYTE1	0x00	RW	Bit[7:0]: Y threshold 3[15:8]
0x561F	Y_TH3_BYTE0	0x00	RW	Bit[7:0]: Y threshold 3[7:0]
0x5621~ 0x56A7	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x56D0	AEC CTRLD0	0x00	RW	Bit[0]: Manual exposure/gain enable for AA mode 0: Auto mode 1: Manual mode
0x56D1	AEC CTRLD1	0x00	RW	Bit[1:0]: Manual_long_gain[9:8] Manual long channel gain
0x56D2	AEC CTRLD2	0x10	RW	Bit[7:0]: Manual_long_gain[7:0] Manual long channel gain
0x56D3	AEC CTRLD3	0x00	RW	Bit[1:0]: Manual_short_gain[9:8] Manual short channel gain
0x56D4	AEC CTRLD4	0x10	RW	Bit[7:0]: Manual_short_gain[7:0] Manual short channel gain
0x56D5	AEC CTRLD5	0x00	RW	Bit[7:0]: Manual_long_exp[31:24] Manual long channel exposure time MSB in unit of row period
0x56D6	AEC CTRLD6	0x00	RW	Bit[7:0]: Manual_long_exp[23:16] Manual long channel exposure time LSB in unit of row period
0x56D7	AEC CTRLD7	0x00	RW	Bit[7:0]: Manual_long_exp[15:8] Manual long channel sub-row exposure time MSB, must be 0 when manual_long_exp[31:16] is greater than 0
0x56D8	AEC CTRLD8	0x00	RW	Bit[7:0]: Manual_long_exp[7:0] Manual long channel sub-row exposure time LSB, must be 0 when manual_long_exp[31:16] is greater than 0
0x56D9	AEC CTRLD9	0x00	RW	Bit[7:0]: Manual_short_exp[31:24] Manual short channel exposure time MSB in unit of row period
0x56DA	AEC CTRLDA	0x00	RW	Bit[7:0]: Manual_short_exp[23:16] Manual short channel exposure time LSB in unit of row period
0x56DB	AEC CTRLDB	0x00	RW	Bit[7:0]: Manual_short_exp[15:8] Manual short channel sub-row exposure time MSB, must be 0 when manual_short_exp[31:16] is greater than 0

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address	register name	default value	R/W	description
0x56DC	AEC CTRLDC	0x00	RW	Bit[7:0]: Manual_short_exp[7:0] Manual short channel sub-row exposure time LSB, must be 0 when manual_short_exp[31:16] is greater than 0
0x5700~ 0x572F	FW_AWB1	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.
0x5730~ 0x5731	RSVD	–	–	Reserved
0x5732~ 0x587A	FW_AWB2	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.
0x587B~ 0x587F	RSVD	–	–	Reserved
0x5880	R_ADVANCED_AWB_ CTRL	0x04	RW	Bit[7:5]: Not used Bit[4:3]: Advanced AWB statistic exposure select 00: L channel 01: S channel 10: VS channel 11: Not used Bit[2]: Advanced AWB simple enable Bit[1]: Advanced AWB statistic ROI enable Bit[0]: Advanced AWB interpolation mode enable
0x5881	R_STAT_RECT_LEFT_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic ROI left coordinate[9:8]
0x5882	R_STAT_RECT_LEFT_L	0x10	RW	Bit[7:0]: Statistic ROI left coordinate[7:0]
0x5883	R_STAT_RECT_TOP_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic ROI top coordinate[9:8]
0x5884	R_STAT_RECT_TOP_L	0x10	RW	Bit[7:0]: Statistic ROI top coordinate[7:0]
0x5885	R_STAT_RECT_RIGHT_H	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Statistic ROI right coordinate[9:8]
0x5886	R_STAT_RECT_RIGHT_L	0x6C	RW	Bit[7:0]: Statistic ROI right coordinate[7:0]
0x5887	R_STAT_RECT_ BOTTOM_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Statistic ROI bottom coordinate[9:8]

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address	register name	default value	R/W	description
0x5888	R_STAT_RECT_ BOTTOM_L	0xC8	RW	Bit[7:0]: Statistic ROI bottom coordinate[7:0]
0x5889	R_STATISTIC_RATE	0x44	RW	Bit[7:4]: X direction statistics rate Bit[3:0]: Y direction statistics rate
0x588A	R_MAX_VALUE_H	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Statistic max value[9:8]
0x588B	R_MAX_VALUE_L	0xE0	RW	Bit[7:0]: Statistic max value[7:0]
0x588C	R_MIN_VALUE_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic min value[9:8]
0x588D	R_MIN_VALUE_L	0x09	RW	Bit[7:0]: Statistic min value[7:0]
0x588E	R_XOFFSET_H	0xFE	RW	Bit[7:0]: XOffset (signed)[15:8]
0x588F	R_XOFFSET_L	0x3D	RW	Bit[7:0]: XOffset (signed)[7:0]
0x5890	R_YOFFSET_H	0xFE	RW	Bit[7:0]: YOffset (signed)[15:8]
0x5891	R_YOFFSET_L	0x42	RW	Bit[7:0]: YOffset (signed)[7:0]
0x5892	R_SCALE_BITS	0x0A	RW	Bit[7:4]: Not used Bit[3:0]: Scale bits
0x5893	R_WEIGHT_TH	0x00	RW	Bit[7:0]: Weight threshold
0x5894~ 0x58A5	RSVD	–	–	Reserved
0x58A6	R_REG3_X_H	0x00	RW	Bit[7:0]: Reg3 x (m_nreg3_x, signed)[15:8]
0x58A7	R_REG3_X_L	0x00	RW	Bit[7:0]: Reg3 x (m_nreg3_x, signed)[7:0]
0x58A8	R_REG3_Y_H	0x00	RW	Bit[7:0]: Reg3 y (m_nreg3_y, signed)[15:8]
0x58A9	R_REG3_Y_L	0x00	RW	Bit[7:0]: Reg3 y (m_nreg3_y, signed)[7:0]
0x58AA	R_REG3_W	0x40	RW	Bit[7:0]: Reg3 w (m_nreg3_w)
0x58AB	R_REG3_H	0x40	RW	Bit[7:0]: Reg3 h (m_nreg3_h)
0x58AC	R_ROW0_WIN_EN	0x1F	RW	Bit[7:5]: Not used Bit[4]: Sub-window 00 enable Bit[3]: Sub-window 01 enable Bit[2]: Sub-window 02 enable Bit[1]: Sub-window 03 enable Bit[0]: Sub-window 04 enable

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address	register name	default value	R/W	description
0x58AD	R_ROW1_WIN_EN	0x1F	RW	Bit[7:5]: Not used Bit[4]: Sub-window 10 enable Bit[3]: Sub-window 11 enable Bit[2]: Sub-window 12 enable Bit[1]: Sub-window 13 enable Bit[0]: Sub-window 14 enable
0x58AE	R_ROW2_WIN_EN	0x1F	RW	Bit[7:5]: Not used Bit[4]: Sub-window 20 enable Bit[3]: Sub-window 21 enable Bit[2]: Sub-window 22 enable Bit[1]: Sub-window 23 enable Bit[0]: Sub-window 24 enable
0x58AF	R_ROW3_WIN_EN	0x1F	RW	Bit[7:5]: Not used Bit[4]: Sub-window 30 enable Bit[3]: Sub-window 31 enable Bit[2]: Sub-window 32 enable Bit[1]: Sub-window 33 enable Bit[0]: Sub-window 34 enable
0x58B0	R_ROW4_WIN_EN	0x1F	RW	Bit[7:5]: Not used Bit[4]: Sub-window 40 enable Bit[3]: Sub-window 41 enable Bit[2]: Sub-window 42 enable Bit[1]: Sub-window 43 enable Bit[0]: Sub-window 44 enable
0x58B1	R_SUB_WIN_WIDTH	0x96	RW	Bit[7:0]: Sub-window width
0x58B2	R_SUB_WIN_HEIGHT	0x68	RW	Bit[7:0]: Sub-window height
0x58B3~ 0x591F	RSVD	–	–	Reserved
0x5980~ 0x5A02	FW_AEC1	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.
0x5A03	HIGHCONVERSIONG	–	–	High Conversion Gain Value This register value must be initialized by user and must not be removed from start up sequence. Default value is random.
0x5A04~ 0x5A24	FW_AEC2	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.

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address	register name	default value	R/W	description
0x5A25	RSVD	–	–	Reserved
0x5A26~ 0x5A2B	FW_AEC3	–	–	Sensor Firmware Registers These register values will be automatically initialized by sensor after powering up. Default value is random.
0x5A2C~ 0x5A2F	RSVD	–	–	Reserved
0x5A0C	HTBLC_TEMP_THRE1	0x46	RW	High Temperature BLC Temperature Start Threshold
0x5A0D	HTBLC_TEMP_THRE2	0x64	RW	High Temperature BLC Temperature End Threshold
0x5A0E	HTBLC_GAIN_THRE1_H	0x00	RW	High Temperature BLC Analog Gain Start Threshold, High Byte
0x5A0F	HTBLC_GAIN_THRE1_L	0x80	RW	High Temperature BLC Analog Gain Start Threshold, Low Byte
0x5A10	HTBLC_GAIN_THRE2_H	0x01	RW	High Temperature BLC Analog Gain End Threshold, High Byte
0x5A11	HTBLC_GAIN_THRE2_L	0x00	RW	High Temperature BLC Analog Gain End Threshold, Low Byte
0x5A12	HT_BLCOFFSETENABLE	0x00	RW	High Temperature BLC Target Offset Enable When register value is 0, function is disabled. Other values mean enabled.
0x5A13	HT_MAX_BLCOFFSET_L	0x70	RW	High Temperature BLC Target Offset BLC Offset for Long Exposure
0x5A14	HT_MAX_BLCOFFSET_S	0x30	RW	High Temperature BLC Target Offset BLC Offset for Short Exposure
0x5A15	HT_MAX_BLCOFFSET_ VS	0x10	RW	High Temperature BLC Target Offset BLC Offset for VS Exposure
0x5A16	HT_GAMMAENABLE	0x01	RW	High Temperature BLC Limit Gamma Function Enable When register value is 0, function is disabled. Other values mean enabled.
0x5A17	HT_GAMMATHRE1	0x04	RW	High Temperature BLC Limit Minimum Gamma Threshold
0x5A18	HT_GAMMATHRE2	0x08	RW	High Temperature BLC Limit Maximum Gamma Threshold
0x5A20	HT_DARKCURRENT THRE1_H	0x00	RW	High Temperature BLC Dark Current Start Threshold, High Byte

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address	register name	default value	R/W	description
0x5A21	HT_DARKCURRENT THRE1_L	0x10	RW	High Temperature BLC Dark Current Start Threshold, Low Byte
0x5A22	HT_DARKCURRENT THRE2_H	0x00	RW	High Temperature BLC Dark Current End Threshold, High Byte
0x5A23	HT_DARKCURRENT THRE2_L	0xA0	RW	High Temperature BLC Dark Current End Threshold, Low Byte
0x5A31~ 0x5A3F	RSVD	–	–	Reserved
0x5A80	R_AEC_AGC_STAT_ TYPE	0x00	RW	Bit[7:1]: Not used Bit[0]: AECAGC statistic type 0: Y channel 1: Max (R,G,B)
0x5A81	R_STAT_WIN_LEFT_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic window left offset[9:8]
0x5A82	R_STAT_WIN_LEFT_L	0x00	RW	Bit[7:0]: Statistic window left offset[7:0]
0x5A83	R_STAT_WIN_RIGHT_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic window right offset[9:8]
0x5A84	R_STAT_WIN_RIGHT_L	0x00	RW	Bit[7:0]: Statistic window right offset[7:0]
0x5A85	R_STAT_WIN_TOP_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic window top offset[9:8]
0x5A86	R_STAT_WIN_TOP_L	0x00	RW	Bit[7:0]: Statistic window top offset[7:0]
0x5A87	R_STAT_WIN_BOTTOM_ H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Statistic window bottom offset[9:8]
0x5A88	R_STAT_WIN_BOTTOM_ L	0x0A	RW	Bit[7:0]: Statistic window bottom offset[7:0]
0x5A89	R_MAX_W_H	0x01	RW	Bit[7:2]: Not used Bit[1]: MaxW[0] Bit[0]: MaxW[1]
0x5A8A	R_MAX_W_0_L	0x20	RW	Bit[7:0]: Max W[0]
0x5A8B	R_MAX_W_1_L	0x00	RW	Bit[7:0]: Max W[1]
0x5A8C	R_MIN_W_0	0x01	RW	Bit[7:0]: Min W[0]
0x5A8D	R_MIN_W_1	0x01	RW	Bit[7:0]: Min W[1]
0x5A8E	R_STAT_DS_RATE	0x04	RW	Bit[7:2]: Not used Bit[2:0]: State down sample rate
0x5A8F	R_POS_W_SHIFT	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PosW shift

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address	register name	default value	R/W	description
0x5A90	R_LOW_LIGHT_THRE	0x00	RW	Bit[7:0]: Threshold to define low light statistics
0x5A91	R_HIGH_LIGHT_THRE	0xF0	RW	Bit[7:0]: Threshold to define high light statistics
0x5A92	R_WIN_LEFT_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Win left [0][9:8]
0x5A93	R_WIN_LEFT_0_L	0x78	RW	Bit[7:0]: Win left [0][7:0]
0x5A94	R_WIN_TOP_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Win top[0][9:8]
0x5A95	R_WIN_TOP_0_L	0x60	RW	Bit[7:0]: Win top[0][7:0]
0x5A96	R_STAT_WIN_WIDTH_0_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Stat win width[0][9:8]
0x5A97	R_STAT_WIN_WIDTH_0_L	0x78	RW	Bit[7:0]: Stat win width[0][7:0]
0x5A98	R_STAT_WIN_HEIGHT_0_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Stat win height[0][9:8]
0x5A99	R_STAT_WIN_HEIGHT_0_L	0x04	RW	Bit[7:0]: Stat win height[0][7:0]
0x5A9A	R_WIN_LEFT_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Win left[1][9:8]
0x5A9B	R_WIN_LEFT_1_L	0x78	RW	Bit[7:0]: Win left[1][7:0]
0x5A9C	R_WIN_TOP_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Win top[1][9:8]
0x5A9D	R_WIN_TOP_1_L	0x60	RW	Bit[7:0]: Win top[1][7:0]
0x5A9E	R_STAT_WIN_WIDTH_1_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Stat win width[1][9:8]
0x5A9F	R_STAT_WIN_WIDTH_1_L	0x78	RW	Bit[7:0]: Stat win width[1][7:0]
0x5AA0	R_STAT_WIN_HEIGHT_1_H	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Stat win height[1][9:8]
0x5AA1	R_STAT_WIN_HEIGHT_1_L	0x04	RW	Bit[7:0]: Stat win height[1][7:0]
0x5AA2	R_WEIGHTS_0	0x11	RW	Bit[7:4]: Weights[0][0] Bit[3:0]: Weights[1][0]
0x5AA3	R_WEIGHTS_1	0x11	RW	Bit[7:4]: Weights[0][1] Bit[3:0]: Weights[1][1]

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address	register name	default value	R/W	description
0x5AA4	R_WEIGHTS_2	0x11	RW	Bit[7:4]: Weights[0][2] Bit[3:0]: Weights[1][2]
0x5AA5	R_WEIGHTS_3	0x11	RW	Bit[7:4]: Weights[0][3] Bit[3:0]: Weights[1][3]
0x5AA6	R_WEIGHTS_4	0x11	RW	Bit[7:4]: Weights[0][4] Bit[3:0]: Weights[1][4]
0x5AA7	R_WEIGHTS_5	0x11	RW	Bit[7:4]: Weights[0][5] Bit[3:0]: Weights[1][5]
0x5AA8	R_WEIGHTS_6	0x11	RW	Bit[7:4]: Weights[0][6] Bit[3:0]: Weights[1][6]
0x5AA9	R_WEIGHTS_7	0x11	RW	Bit[7:4]: Weights[0][7] Bit[3:0]: Weights[1][7]
0x5AAA	R_WEIGHTS_8	0x11	RW	Bit[7:4]: Weights[0][8] Bit[3:0]: Weights[1][8]
0x5AAB	R_WEIGHTS_9	0x11	RW	Bit[7:4]: Weights[0][9] Bit[3:0]: Weights[1][9]
0x5AAC	R_WEIGHTS_10	0x11	RW	Bit[7:4]: Weights[0][10] Bit[3:0]: Weights[1][10]
0x5AAD	R_WEIGHTS_11	0x11	RW	Bit[7:4]: Weights[0][11] Bit[3:0]: Weights[1][11]
0x5AAE	R_WEIGHTS_12	0x11	RW	Bit[7:4]: Weights[0][12] Bit[3:0]: Weights[1][12]
0x5AAF	R_ROI_LEFT_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI left[0][9:8]
0x5AB0	R_ROI_LEFT_0_L	0x00	RW	Bit[7:0]: ROI left[0][7:0]
0x5AB1	R_ROI_TOP_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI top[0][9:8]
0x5AB2	R_ROI_TOP_0_L	0x00	RW	Bit[7:0]: ROI top[0][7:0]
0x5AB3	R_ROI_RIGHT_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI right[0][9:8]
0x5AB4	R_ROI_RIGHT_0_L	0x00	RW	Bit[7:0]: ROI right[0][7:0]
0x5AB5	R_ROI_BOTTOM_0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI bottom[0][9:8]
0x5AB6	R_ROI_BOTTOM_0_L	0x00	RW	Bit[7:0]: ROI bottom[0][7:0]
0x5AB7	R_ROI_WEIGHTS_0	0x11	RW	Bit[7:4]: ROI weights[0][0] Bit[3:0]: ROI weights[0][1]

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address	register name	default value	R/W	description
0x5AB8	R_ROI_LEFT_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI left[1][9:8]
0x5AB9	R_ROI_LEFT_1_L	0x00	RW	Bit[7:0]: ROI left[1][7:0]
0x5ABA	R_ROI_TOP_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI top[1][9:8]
0x5ABB	R_ROI_TOP_1_L	0x00	RW	Bit[7:0]: ROI top[1][7:0]
0x5ABC	R_ROI_RIGHT_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI right[1][9:8]
0x5ABD	R_ROI_RIGHT_1_L	0x00	RW	Bit[7:0]: ROI right[1][7:0]
0x5ABE	R_ROI_BOTTOM_1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: ROI bottom[1][9:8]
0x5ABF	R_ROI_BOTTOM_1_L	0x00	RW	Bit[7:0]: ROI bottom[1][7:0]
0x5AC0	R_ROI_WEIGHTS_1	0x11	RW	Bit[7:4]: ROI weights[1][0] Bit[3:0]: ROI weights[1][1]
0x5AC1	R_ROI_SHIFT	0x00	RW	Bit[7:4]: Not used Bit[3:2]: ROI shift[0] Bit[1:0]: ROI shift[1]
0x5AC2	R_BLACK_THRE1_0_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black threshold1[0] byte 2
0x5AC3	R_BLACK_THRE1_0_B1	0x01	RW	Bit[7:0]: Black threshold1[0] byte 1
0x5AC4	R_BLACK_THRE1_0_B0	0x00	RW	Bit[7:0]: Black threshold1[0] byte 0
0x5AC5	R_BLACK_THRE2_0_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black threshold2[0] byte 2
0x5AC6	R_BLACK_THRE2_0_B1	0x08	RW	Bit[7:0]: Black threshold2[0] byte 1
0x5AC7	R_BLACK_THRE2_0_B0	0x00	RW	Bit[7:0]: Black threshold2[0] byte 0
0x5AC8	R_BLACK_WEIGHT1_0	0x10	RW	Bit[7]: Not used Bit[6:0]: Black weight1[0]
0x5AC9	R_BLACK_WEIGHT2_0	0x14	RW	Bit[7]: Not used Bit[6:0]: Black weight2[0]
0x5ACA	R_SATURATE_THRE1_0_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate threshold1[0] byte 2
0x5ACB	R_SATURATE_THRE1_0_B1	0x02	RW	Bit[7:0]: Saturate threshold1[0] byte 1

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address	register name	default value	R/W	description
0x5ACC	R_SATURATE_THRE1_0_B0	0x00	RW	Bit[7:0]: Saturate threshold1[0] byte 0
0x5ACD	R_SATURATE_THRE2_0_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate threshold2[0] byte 2
0x5ACE	R_SATURATE_THRE2_0_B1	0x04	RW	Bit[7:0]: Saturate threshold2[0] byte 1
0x5ACF	R_SATURATE_THRE2_0_B0	0x00	RW	Bit[7:0]: Saturate threshold2[0] byte 0
0x5AD0	R_SATURATE_WEIGHT1_0	0x08	RW	Bit[7]: Not used Bit[6:0]: Saturate weight1[0]
0x5AD1	R_SATURATE_WEIGHT2_0	0x12	RW	Bit[7]: Not used Bit[6:0]: Saturate weight2[0]
0x5AD2	R_BLACK_THRE1_1_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black threshold1[1] byte 2
0x5AD3	R_BLACK_THRE1_1_B1	0x04	RW	Bit[7:0]: Black threshold1[1] byte 1
0x5AD4	R_BLACK_THRE1_1_B0	0x00	RW	Bit[7:0]: Black threshold1[1] byte 0
0x5AD5	R_BLACK_THRE2_1_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Black threshold2[1] byte 2
0x5AD6	R_BLACK_THRE2_1_B1	0x10	RW	Bit[7:0]: Black threshold2 [1] byte 1
0x5AD7	R_BLACK_THRE2_1_B0	0x00	RW	Bit[7:0]: Black threshold2[1] byte 0
0x5AD8	R_BLACK_WEIGHT1_1	0x08	RW	Bit[7]: Not used Bit[6:0]: Black weight1[1]
0x5AD9	R_BLACK_WEIGHT2_1	0x12	RW	Bit[7]: Not used Bit[6:0]: Black weight2[1]
0x5ADA	R_SATURATE_THRE1_1_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate threshold1[1] byte 2
0x5ADB	R_SATURATE_THRE1_1_B1	0x01	RW	Bit[7:0]: Saturate threshold1[1] byte 1
0x5ADC	R_SATURATE_THRE1_1_B0	0x00	RW	Bit[7:0]: Saturate threshold1[1] byte 0
0x5ADD	R_SATURATE_THRE2_1_B2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Saturate threshold2[1] byte 2
0x5ADE	R_SATURATE_THRE2_1_B1	0x08	RW	Bit[7:0]: Saturate threshold2[1] byte 1

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address	register name	default value	R/W	description
0x5ADF	R_SATURATE_THRE2_1_B0	0x00	RW	Bit[7:0]: Saturate threshold2[1] byte 0
0x5AE0	R_SATURATE_WEIGHT1_1	0x10	RW	Bit[7]: Not used Bit[6:0]: Saturate weight1[1]
0x5AE1	R_SATURATE_WEIGHT2_1	0x14	RW	Bit[7]: Not used Bit[6:0]: Saturate weight2[1]
0x5AE2	R_MEAN_Y_0	–	R	Bit[7:0]: Mean Y[0]
0x5AE3	R_MEAN_Y_1	–	R	Bit[7:0]: Mean Y[1]
0x5B00	STRETCH_CTRL0_O	0x09	RW	Bit[7:4]: Not used Bit[3:2]: Stretch minimum register, Real stretch minimum value is: 00: 1024 01: 2048 10: 4096 11: 8192 Bit[1]: Stretch manual 0: Disable 1: Enable Bit[0]: Stretch auto 0: Disable 1: Enable
0x5B01	STRETCH_CTRL1_0_O	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Stretch minimum lowlevel
0x5B02	STRETCH_CTRL1_1_O	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Stretch maximum lowlevel
0x5B03	STRETCH_CTRL2_O	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Stretch minimum highlevel
0x5B04	STRETCH_CTRL3_O	0x41	RW	Bit[7:4]: Stretch step2 value Bit[3:0]: Stretch step1 value
0x5B05	STRETCH_CTRL4_O	0x10	RW	Bit[7:0]: Stretch low level initial value[7:0]
0x5B06	STRETCH_CTRL5_O	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Stretch high level initial value[9:8]
0x5B07	STRETCH_CTRL6_O	0xFF	RW	Bit[7:0]: Stretch high level initial value[7:0]
0x5B08	STRETCH_CTRL7_O	0x10	RW	Bit[7:0]: Current low level manual value[7:0]
0x5B09	STRETCH_CTRL8_O	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Current high level manual value[9:8]
0x5B0A	STRETCH_CTRL9_O	0xFF	RW	Bit[7:0]: Current high level manual value[7:0]
0x5B0B	STRETCH_CTRLA_O	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Stretch threshold[17:16]

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address	register name	default value	R/W	description
0x5B0C	STRETCH_CTRLB_O	0x3B	RW	Bit[7:0]: Stretch threshold 1[15:8]
0x5B0D	STRETCH_CTRLC_O	0xC4	RW	Bit[7:0]: Stretch threshold 1[7:0]
0x5B0E	STRETCH_CTRLD_O	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Stretch threshold 2[17:16]
0x5B0F	STRETCH_CTRLE_O	0x3B	RW	Bit[7:0]: Stretch threshold 2[15:8]
0x5B10	STRETCH_CTRLF_O	0xC4	RW	Bit[7:0]: Stretch threshold 2[7:0]
0x5B11	CUR_LOWLVL_I	–	R	Bit[7:0]: Current low level[7:0]
0x5B12	CUR_HIGHLVL_H_I	–	R	Bit[7:2]: Not used Bit[1:0]: Current high level[9:8]
0x5B13	CUR_HIGHLVL_L_I	–	R	Bit[7:0]: Current high level[7:0]
0x5B14	STRETCH_GAIN_H_I	–	R	Bit[7:1]: Not used Bit[0]: Stretch gain value[8]
0x5B15	STRETCH_GAIN_L_I	–	R	Bit[7:0]: Stretch gain value[7:0]
0x5B80	R_L_DPC_CTRL00	0x18	RW	For Long Exposure Channel Bit[7]: Tail type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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address	register name	default value	R/W	description
0x5B81	R_L_DPC_CTRL01	0xDF	RW	For Long Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5B82	R_L_DPC_CTRL02	0xFF	RW	For Long Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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address	register name	default value	R/W	description
0x5B83	R_L_WTHREGLIST1	0x08	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5B84	R_L_WTHREGLIST2	0x20	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5B85	R_L_THRE1	0x10	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but less effective of recovering defect
0x5B86	R_L_THRE2	0x20	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5B87	R_L_THRE3	0x10	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine high frequency area where DPC will keep fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5B88	R_L_THRE4	0x18	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single white/black pixel
0x5B89	R_L_WTHRE_LIST0	0x08	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode

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address	register name	default value	R/W	description
0x5B8A	R_L_WTHRE_LIST1	0x04	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x5B8B	R_L_WTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x5B8C	R_L_WTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x5B8D	R_L_BTHRE_LIST0	0x0C	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 0 in auto mode
0x5B8E	R_L_BTHRE_LIST1	0x06	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 1 in auto mode
0x5B8F	R_L_BTHRE_LIST2	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 2 in auto mode
0x5B90	R_L_BTHRE_LIST3	0x02	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 3 in auto mode
0x5B91	R_L_SAT	0xFF	RW	For Long Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5B92	R_L_VB_GAIN_TH1	0x07	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1
0x5B93	R_L_VB_GAIN_TH2	0x03	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x5B94	R_L_SMOOTH_GLIST0	0x03	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x5B95	R_L_SMOOTH_GLIST1	0x07	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1

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address	register name	default value	R/W	description
0x5B96	R_L_SMOOTH_GLIST2	0x0F	RW	For Long Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x5B97~ 0x5B98	NOT USED	–	–	Not Used
0x5B99	R_L_UNSAT	0xF0	RW	For Long Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5B9A	R_L_TTHRE	0x08	RW	For Long Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x5BA0	R_S_DPC_CTRL00	0x18	RW	For Short Exposure Channel Bit[7]: Tail type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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address	register name	default value	R/W	description
0x5BA1	R_S_DPC_CTRL01	0xDF	RW	For Short Exposure Channel Bit[7]: Set threshold for T-cluster 0: Automatically 1: Manually Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5BA2	R_S_DPC_CTRL02	0xFF	RW	For Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed: 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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address	register name	default value	R/W	description
0x5BA3	R_S_WTHREGLIST1	0x08	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5BA4	R_S_WTHREGLIST2	0x20	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5BA5	R_S_THRE1	0x10	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x5BA6	R_S_THRE2	0x20	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5BA7	R_S_THRE3	0x10	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where DPC will keep fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5BA8	R_S_THRE4	0x18	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x5BA9	R_S_WTHRE_LIST0	0x08	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode

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address	register name	default value	R/W	description
0x5BAA	R_S_WTHRE_LIST1	0x04	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x5BAB	R_S_WTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x5BAC	R_S_WTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x5BAD	R_S_BTHRE_LIST0	0x0C	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 0 in auto mode
0x5BAE	R_S_BTHRE_LIST1	0x06	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 1 in auto mode
0x5BAF	R_S_BTHRE_LIST2	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 2 in auto mode
0x5BB0	R_S_BTHRE_LIST3	0x02	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 3 in auto mode
0x5BB1	R_S_SAT	0xFF	RW	For Short Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5BB2	R_S_VB_GAIN_TH1	0x07	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1
0x5BB3	R_S_VB_GAIN_TH2	0x03	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x5BB4	R_S_SMOOTH_GLIST0	0x03	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x5BB5	R_S_SMOOTH_GLIST1	0x07	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1

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address	register name	default value	R/W	description
0x5BB6	R_S_SMOOTH_GLIST2	0x0F	RW	For Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x5BB7~ 0x5BB8	NOT USED	–	–	Not Used
0x5BB9	R_S_UNSAT	0xF0	RW	For Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5BBA	R_S_TTHRE	0x08	RW	For Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x5BC0	R_VS_DPC_CTRL00	0x18	RW	For Very Short Exposure Channel Bit[7]: Tail type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[6]: Saturation type cross cluster correction enable Works only when cross cluster correction is enabled 0: Disable 1: Enable Bit[5]: Cross cluster correction enable Bit[4]: Horizontal same color plane couplet correction enable 0: Disable 1: Enable Bit[3]: Horizontal couplet correction enable 0: Disable 1: Enable Bit[2]: Not used Bit[1]: r_bwsnr_en Bit[0]: Manual threshold mode 0: Auto mode in which defect pixel threshold is automatically adjusted based on analog gain 1: Manual mode in which defect pixel threshold is set manually by register

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table A-1 sensor control registers (sheet 86 of 112)

address	register name	default value	R/W	description
0x5BC1	R_VS_DPC_CTRL01	0xDF	RW	For Very Short Exposure Channel Bit[7]: Manually set threshold for T-cluster Bit[6]: r_comp_en Bit[5]: Vertical black pixel detection 0: Disable 1: Enable Bit[4]: Color line detection 0: Always disable 1: Enable color line detection in manual mode Bit[3]: Additional detection of defect pixel of cross-cluster in current line 0: Disable 1: Enable Bit[2]: T-cluster detection 0: Disable 1: Enable Bit[1:0]: Padding method of edge pixels 00: Pad with 0 01: Pad with 255 10: Pad with (255+1)/2 11: Pad with nearby same channel pixel This option will affect defect pixel detection of boundary pixels
0x5BC2	R_VS_DPC_CTRL02	0xFF	RW	For Very Short Exposure Channel Bit[7]: White defect pixel detection 0: Disable 1: Enable Bit[6]: Black defect pixel detection 0: Disable 1: Enable Bit[5:4]: Pixel number threshold for detection of cross-cluster Bit[3:2]: Pixel number threshold for detection of T-cluster Bit[1:0]: Number of vertical connected white pixels removed 00: Remove upper one white pixel 01: Remove two vertical white pixels 10: Remove three or less vertical connected white pixel

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table A-1 sensor control registers (sheet 87 of 112)

address	register name	default value	R/W	description
0x5BC3	R_VS_WTHREGLIST1	0x08	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting white pixel in manual More white pixels will be removed with smaller threshold. Gain threshold 1 for defect pixel threshold calculation in auto mode
0x5BC4	R_VS_WTHREGLIST2	0x20	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value for detecting black pixel in manual mode More black pixels will be removed with smaller threshold. Gain threshold 2 for defect pixel threshold calculation in auto mode
0x5BC5	R_VS_THRE1	0x10	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold value used in recovery of defect pixel for long channel The bigger the value, the more details retained, but the less effective of recovering defect
0x5BC6	R_VS_THRE2	0x20	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for registering defect pixel to detect cross cluster for long channel The greater the threshold, the more defect pixels will be removed
0x5BC7	R_VS_THRE3	0x10	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine high frequency area where the DPC will keep the fine details for long channel The greater the threshold, the more details will be removed by DPC
0x5BC8	R_VS_THRE4	0x18	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Threshold for detecting horizontal couplet for long channel This threshold should be greater than the threshold for single while/black pixel
0x5BC9	R_VS_WTHRE_LIST0	0x08	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 0 in auto mode

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table A-1 sensor control registers (sheet 88 of 112)

address	register name	default value	R/W	description
0x5BCA	R_VS_WTHRE_LIST1	0x04	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 1 in auto mode
0x5BCB	R_VS_WTHRE_LIST2	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 2 in auto mode
0x5BCC	R_VS_WTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: White pixel threshold 3 in auto mode
0x5BCD	R_VS_BTHRE_LIST0	0x0C	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 0 in auto mode
0x5BCE	R_VS_BTHRE_LIST1	0x06	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 1 in auto mode
0x5BCF	R_VS_BTHRE_LIST2	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 2 in auto mode
0x5BD0	R_VS_BTHRE_LIST3	0x02	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Black pixel threshold 3 in auto mode
0x5BD1	R_VS_SAT	0xFF	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of center pixel for saturation type of cross cluster To qualify a saturation type of cross cluster, center pixel must be greater than this threshold
0x5BD2	R_VS_VB_GAIN_TH1	0x07	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 1
0x5BD3	R_VS_VB_GAIN_TH2	0x03	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Vertical black pixel detection threshold 2
0x5BD4	R_VS_SMOOTH_ GLIST0	0x03	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 0
0x5BD5	R_VS_SMOOTH_ GLIST1	0x07	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 1

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address	register name	default value	R/W	description
0x5BD6	R_VS_SMOOTH_ GLIST2	0x0F	RW	For Very Short Exposure Channel Bit[7]: Not used Bit[6:0]: Smooth gain list 2
0x5BD7~ 0x5BD8	NOT USED	–	–	Not Used
0x5BD9	R_VS_UNSAT	0xF0	RW	For Very Short Exposure Channel Bit[7:0]: Threshold of un-saturation level for detection of cross-cluster and T-cluster
0x5BDA	R_VS_TTHRE	0x08	RW	For Very Short Exposure Channel Bit[7:0]: Threshold to determine a cross-cluster and T-cluster
0x5BE0~ 0x5BF7	RSVD	–	–	Reserved
0x5C00	DNS_CTRL0	0x0D	RW	Bit[7:6]: Not used Bit[5:2]: raw_dns_noise_yslop Bit[1]: raw_dns_para_man_en 0: Manual mode 1: Auto mode Bit[0]: Enable G pixel in process
0x5C01	DNS_NOISE_LIST_0	0x04	RW	Bit[7:0]: Register for RAW de-noise noiselist0
0x5C02	DNS_NOISE_LIST_1	0x08	RW	Bit[7:0]: Register for RAW de-noise noiselist1
0x5C03	DNS_NOISE_LIST_2	0x10	RW	Bit[7:0]: Register for RAW de-noise noiselist2
0x5C04	DNS_NOISE_LIST_3	0x18	RW	Bit[7:0]: Register for RAW de-noise noiselist3
0x5C05	DNS_NOISE_LIST_4	0x20	RW	Bit[7:0]: Register for RAW de-noise noiselist4
0x5C06	DNS_NOISE_LIST_5	0x30	RW	Bit[7:0]: Register for RAW de-noise noiselist5
0x5C07	DNS_NOISE_LIST_6	0x40	RW	Bit[7:0]: Register for RAW de-noise noiselist6
0x5C08	DNS_NOISE_LIST_7	0x40	RW	Bit[7:0]: Register for RAW de-noise noiselist7
0x5C09	DNS_MAX_EDGETHRE	0xFF	RW	Bit[7:0]: Maximum edge threshold
0x5C0A	DNS_NOISE_MAN	0x08	RW	Bit[7:0]: Manual noise level
0x5C0B	DNS_EDGETHRE_MAN	0x18	RW	Bit[7:0]: Manual edge threshold

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address	register name	default value	R/W	description
0x5C0C	DNS_NOISE	–	R	Bit[7:0]: Noise result according to real gain
0x5C0D	DNS_EDGETHRE	–	R	Bit[7:0]: Noise result according to real gain
0x5C80	R_CIP_CTRL_0	0x80	RW	Bit[7:4]: Noise Y slope Bit[3:0]: Local sharpen
0x5C81	R_CIP_CTRL_1	0x00	RW	Bit[7:5]: Not used Bit[4:1]: GbGr shift Bit[0]: GbGr remove enable
0x5C82	R_CIP_NOISE_LIST_0	0x00	RW	Bit[7:0]: Noise List[0]
0x5C83	R_CIP_NOISE_LIST_1	0x00	RW	Bit[7:0]: Noise List[1]
0x5C84	R_CIP_NOISE_LIST_2	0x00	RW	Bit[7:0]: Noise List[2]
0x5C85	R_CIP_NOISE_LIST_3	0x00	RW	Bit[7:0]: Noise List[3]
0x5C86	R_CIP_NOISE_LIST_4	0x00	RW	Bit[7:0]: Noise List[4]
0x5C87	R_CIP_NOISE_LIST_5	0x00	RW	Bit[7:0]: Noise List[5]
0x5C88	R_CIP_NOISE_LIST_6	0x00	RW	Bit[7:0]: Noise List[6]
0x5C89	R_CIP_NOISE_LIST_7	0x00	RW	Bit[7:0]: Noise List[7]
0x5C8A	R_CIP_MIN_SHARPEN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: Minimum sharpen
0x5C8B	R_CIP_MAX_SHARPEN	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: Maximum sharpen
0x5C8C	R_CIP_MIN_DETAIL	0x08	RW	Bit[7:0]: Minimum detail
0x5C8D	R_CIP_MAX_DETAIL	0x0C	RW	Bit[7:0]: Maximum detail
0x5C8E	R_CIP_MIN_SHARPEN_ GAIN	0x02	RW	Bit[7:0]: Minimum sharpen gain
0x5C8F	R_CIP_MAX_SHARPEN_ GAIN	0x10	RW	Bit[7:0]: Maximum sharpen gain
0x5C90	R_CIP_CTRL_2	0x60	RW	Bit[7]: Not used Bit[6]: Anti aliasing Bit[5]: FixH binning enable Bit[4]: CIP option Bit[3:2]: Binning pattern Bit[1:0]: Binning mode
0x5C91	R_CIP_EOF_DELAY	0x28	RW	Bit[7]: Not used Bit[6:0]: Number of EOF signal delay cycles
0x5C92	R_CIP_AF_FILTER_ COEF_0	0x00	RW	Bit[7:0]: AF filter coefficient[0]

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address	register name	default value	R/W	description
0x5C93	R_CIP_AF_FILTER_COEF_1	0x00	RW	Bit[7:0]: AF filter coefficient[1]
0x5C94	R_CIP_AF_FILTER_COEF_2	0x00	RW	Bit[7:0]: AF filter coefficient[2]
0x5C95	R_CIP_AF_FILTER_COEF_3	0x00	RW	Bit[7:0]: AF filter coefficient[3]
0x5C96	R_CIP_CTRL_3	0x10	RW	Bit[7]: Anti flickering enable Bit[6:5]: Reserved Bit[4:0]: Sharpen V coefficient
0x5D00	R_CMX_CTRL0_O	0x03	RW	Bit[7:4]: Not used Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D01	R_CMX_CTRL1_O	0xF2	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in day color temperature mode
0x5D02	R_CMX_CTRL2_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in day color temperature mode
0x5D03	R_CMX_CTRL3_O	0x39	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in day color temperature mode
0x5D04	R_CMX_CTRL4_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B channel in day color temperature mode
0x5D05	R_CMX_CTRL5_O	0xAF	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in day color temperature mode
0x5D06	R_CMX_CTRL6_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in day color temperature mode

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address	register name	default value	R/W	description
0x5D07	R_CMX_CTRL7_O	0x42	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in day color temperature mode
0x5D08	R_CMX_CTRL8_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in day color temperature mode
0x5D09	R_CMX_CTRL9_O	0x99	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in day color temperature mode
0x5D0A	R_CMX_CTRLA_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in day color temperature mode
0x5D0B	R_CMX_CTRLB_O	0x00	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in day color temperature mode
0x5D0C	R_CMX_CTRLC_O	0x06	RW	Bit[7:4]: Not used Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D0D	R_CMX_CTRLD_O	0x80	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in A color temperature mode
0x5D0E	R_CMX_CTRLE_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in A color temperature mode
0x5D0F	R_CMX_CTRLF_O	0x5B	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in A color temperature mode

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address	register name	default value	R/W	description
0x5D10	R_CMX_CTRL10_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B channel in A color temperature mode
0x5D11	R_CMX_CTRL11_O	0x10	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in A color temperature mode
0x5D12	R_CMX_CTRL12_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in A color temperature mode
0x5D13	R_CMX_CTRL13_O	0xDD	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in A color temperature mode
0x5D14	R_CMX_CTRL14_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in A color temperature mode
0x5D15	R_CMX_CTRL15_O	0x7F	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in A color temperature mode
0x5D16	R_CMX_CTRL16_O	0x03	RW	Bit[7:4]: Not used Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in A color temperature mode
0x5D17	R_CMX_CTRL17_O	0x22	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in A color temperature mode
0x5D18	R_CMX_CTRL18_O	0x05	RW	Bit[7:4]: Not used Bit[3:0]: CMX00[11:8] Highest 4 bits of color matrix for G channel in CWF color temperature mode

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address	register name	default value	R/W	description
0x5D19	R_CMX_CTRL19_O	0x46	RW	Bit[7:0]: CMX00[7:0] Lowest 8 bits of color matrix for G channel in CWF color temperature mode
0x5D1A	R_CMX_CTRL1A_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX01[11:8] Highest 4 bits of color matrix for R channel in CWF color temperature mode
0x5D1B	R_CMX_CTRL1B_O	0x53	RW	Bit[7:0]: CMX01[7:0] Lowest 8 bits of color matrix for R channel in CWF color temperature mode
0x5D1C	R_CMX_CTRL1C_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX10[11:8] Highest 4 bits of color matrix for B Channel in CWF color temperature mode
0x5D1D	R_CMX_CTRL1D_O	0x08	RW	Bit[7:0]: CMX10[7:0] Lowest 8 bits of color matrix for B channel in CWF color temperature mode
0x5D1E	R_CMX_CTRL1E_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX11[11:8] Highest 4 bits of color matrix for R channel in CWF color temperature mode
0x5D1F	R_CMX_CTRL1F_O	0x43	RW	Bit[7:0]: CMX11[7:0] Lowest 8 bits of color matrix for R channel in CWF color temperature mode
0x5D20	R_CMX_CTRL20_O	0x00	RW	Bit[7:4]: Not used Bit[3:0]: CMX20[11:8] Highest 4 bits of color matrix for B channel in CWF color temperature mode
0x5D21	R_CMX_CTRL21_O	0x81	RW	Bit[7:0]: CMX20[7:0] Lowest 8 bits of color matrix for B channel in CWF color temperature mode

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address	register name	default value	R/W	description
0x5D22	R_CMX_CTRL22_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: CMX21[11:8] Highest 4 bits of color matrix for G channel in CWF color temperature mode
0x5D23	R_CMX_CTRL23_O	0x55	RW	Bit[7:0]: CMX21[7:0] Lowest 8 bits of color matrix for G channel in CWF color temperature mode
0x5D24	R_CMX_CTRL24_O	0x01	RW	Bit[7:5]: Not used Bit[4]: CMX BR gain manual Bit[3:0]: AWB B gain[11:8] 0: Disable 1: Enable
0x5D25	R_CMX_CTRL25_O	0x00	RW	Bit[7:0]: AWB B gain[7:0]
0x5D26	R_CMX_CTRL26_O	0x01	RW	Bit[7:4]: Not used Bit[3:0]: AWB R gain[11:8]
0x5D27	R_CMX_CTRL27_O	0x00	RW	Bit[7:0]: AWB R gain[7:0]
0x5D28	R_CMX_CTRL28_O	0x00	RW	CMX Color Temperature Threshold Bit[7:2]: Not used Bit[1:0]: List_0[9:8] for day color temperature mode
0x5D29	R_CMX_CTRL29_O	0x72	RW	CMX Color Temperature Threshold Bit[7:0]: List_0[7:0] for day color temperature mode
0x5D2A	R_CMX_CTRL2A_O	0x00	RW	CMX Color Temperature Threshold Bit[7:2]: Not used Bit[1:0]: List_1[9:8] for CWF color temperature mode
0x5D2B	R_CMX_CTRL2B_O	0xBA	RW	CMX Color Temperature Threshold Bit[7:0]: List_1[7:0] for CWF color temperature mode
0x5D2C	R_CMX_CTRL2C_O	0x01	RW	CMX Color Temperature Threshold Bit[7:2]: Not used Bit[1:0]: List_2[9:8] for A color temperature mode
0x5D2D	R_CMX_CTRL2D_O	0x37	RW	CMX Color Temperature Threshold Bit[7:0]: List_2[7:0] for A color temperature mode
0x5D2E	R_CMX_CTRL2E_O	0x02	RW	Six Coefficient Signs in Day Color Temperature Mode, 0 Indicates Negative

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address	register name	default value	R/W	description
0x5D2F	R_CMX_CTRL2F_O	0x00	RW	Six Coefficient Signs in A Color Temperature Mode, 0 Indicates Negative
0x5D30	R_CMX_CTRL30_O	0x00	RW	Six Coefficient Signs in CWF Color Temperature Mode, 0 Indicates Negative
0x5D31	R_CMX_CTRL31_O	0x01	RW	Bit[7:2]: Not used Bit[1]: CT based color matrix 0: Always use single matrix D in all color temperatures 1: Enable CT based color matrix Bit[0]: CMX auto factor enable signal 0: Do not reduce color saturation when large sensor gain 1: Automatically reduce color saturation when large sensor gain, see 0x5D32 and 0x5D33
0x5D32	R_CMX_CTRL32_O	0x64	RW	CMX Maximum Factor Value Factor used when sensor gain is below CMX minimum gain value in register 0x5D34
0x5D33	R_CMX_CTRL33_O	0x64	RW	CMX Minimum Factor Value Factor used when sensor gain is exceeding CMX maximum gain value in register 0x5D35
0x5D34	R_CMX_CTRL34_O	0x07	RW	CMX Minimum Gain Value
0x5D35	R_CMX_CTRL35_O	0x15	RW	CMX Maximum Gain Value
0x5D36	ABS_CMX00_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX00[11:8] Read register of color matrix for G channel
0x5D37	ABS_CMX00_L_I	–	R	Bit[7:0]: CMX00[7:0] Read register of color matrix for G channel
0x5D38	ABS_CMX01_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX01[11:8] Read register of color matrix for R channel
0x5D39	ABS_CMX01_L_I	–	R	Bit[7:0]: CMX01[7:0] Read register of color matrix for R channel
0x5D3A	ABS_CMX10_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX10[11:8] Read register of color matrix for B channel

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address	register name	default value	R/W	description
0x5D3B	ABS_CMX10_L_I	–	R	Bit[7:0]: CMX10[7:0] Read register of color matrix for B channel
0x5D3C	ABS_CMX11_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX11[11:8] Read register of color matrix for R channel
0x5D3D	ABS_CMX11_L_I	–	R	Bit[7:0]: CMX11[7:0] Read register of color matrix for R channel
0x5D3E	ABS_CMX20_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX20[11:8] Read register of color matrix for B channel
0x5D3F	ABS_CMX20_L_I	–	R	Bit[7:0]: CMX20[7:0] Read register color matrix for B channel
0x5D40	ABS_CMX21_H_I	–	R	Bit[7:4]: Not used Bit[3:0]: CMX21[11:8] Read register of color matrix for G channel
0x5D41	ABS_CMX21_L_I	–	R	Bit[7:0]: CMX21[7:0] Read register of color matrix for G channel
0x5D42	SIGN_CMX	–	R	Read Register for Matrix Six Value Signs, 0 Indicates Negative
0x5D80	R_Y_LIST_00_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[0][9:8]
0x5D81	R_Y_LIST_00_AUTO_L	0x0E	RW	Bit[7:0]: Gamma curve Y list[0][7:0]
0x5D82	R_Y_LIST_01_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[1][9:8]
0x5D83	R_Y_LIST_01_AUTO_L	0x1A	RW	Bit[7:0]: Gamma curve Y list[1][7:0]
0x5D84	R_Y_LIST_02_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[2][9:8]
0x5D85	R_Y_LIST_02_AUTO_L	0x31	RW	Bit[7:0]: Gamma curve Y list[2][7:0]
0x5D86	R_Y_LIST_03_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[3][9:8]
0x5D87	R_Y_LIST_03_AUTO_L	0x5A	RW	Bit[7:0]: Gamma curve Y list[3][7:0]

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address	register name	default value	R/W	description
0x5D88	R_Y_LIST_04_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[4][9:8]
0x5D89	R_Y_LIST_04_AUTO_L	0x69	RW	Bit[7:0]: Gamma curve Y list[4][7:0]
0x5D8A	R_Y_LIST_05_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[5][9:8]
0x5D8B	R_Y_LIST_05_AUTO_L	0xD7	RW	Bit[7:0]: Gamma curve Y list[5][7:0]
0x5D8C	R_Y_LIST_06_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[6][9:8]
0x5D8D	R_Y_LIST_06_AUTO_L	0xE8	RW	Bit[7:0]: Gamma curve Y list[6][7:0]
0x5D8E	R_Y_LIST_07_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[7][9:8]
0x5D8F	R_Y_LIST_07_AUTO_L	0x88	RW	Bit[7:0]: Gamma curve Y list[7][7:0]
0x5D90	R_Y_LIST_08_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[8][9:8]
0x5D91	R_Y_LIST_08_AUTO_L	0x8F	RW	Bit[7:0]: Gamma curve Y list[8][7:0]
0x5D92	R_Y_LIST_09_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[9][9:8]
0x5D93	R_Y_LIST_09_AUTO_L	0x96	RW	Bit[7:0]: Gamma curve Y list[9][7:0]
0x5D94	R_Y_LIST_10_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[10][9:8]
0x5D95	R_Y_LIST_10_AUTO_L	0xA3	RW	Bit[7:0]: Gamma curve Y list[10][7:0]
0x5D96	R_Y_LIST_11_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[11][9:8]
0x5D97	R_Y_LIST_11_AUTO_L	0xAF	RW	Bit[7:0]: Gamma curve Y list[11][7:0]
0x5D98	R_Y_LIST_12_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[12][9:8]
0x5D99	R_Y_LIST_12_AUTO_L	0xC4	RW	Bit[7:0]: Gamma curve Y list[12][7:0]
0x5D9A	R_Y_LIST_13_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[13][9:8]
0x5D9B	R_Y_LIST_13_AUTO_L	0xB0	RW	Bit[7:0]: Gamma curve Y list[13][7:0]
0x5D9C	R_Y_LIST_14_AUTO_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Gamma curve Y list[14][9:8]
0x5D9D	R_Y_LIST_14_AUTO_L	0xD0	RW	Bit[7:0]: Gamma curve Y list[14][7:0]
0x5D9E	R_Y_LIST_00_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[0][9:8]

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address	register name	default value	R/W	description
0x5D9F	R_Y_LIST_00_MANUAL_L	0x04	RW	Bit[7:0]: Manual gamma curve Y list[0][7:0]
0x5DA0	R_Y_LIST_01_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[1][9:8]
0x5DA1	R_Y_LIST_01_MANUAL_L	0x08	RW	Bit[7:0]: Manual gamma curve Y list[1][7:0]
0x5DA2	R_Y_LIST_02_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[2][9:8]
0x5DA3	R_Y_LIST_02_MANUAL_L	0x10	RW	Bit[7:0]: Manual gamma curve Y list[2][7:0]
0x5DA4	R_Y_LIST_03_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[3][9:8]
0x5DA5	R_Y_LIST_03_MANUAL_L	0x20	RW	Bit[7:0]: Manual gamma curve Y list[3][7:0]
0x5DA6	R_Y_LIST_04_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[4][9:8]
0x5DA7	R_Y_LIST_04_MANUAL_L	0x28	RW	Bit[7:0]: Manual gamma curve Y list[4][7:0]
0x5DA8	R_Y_LIST_05_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[5][9:8]
0x5DA9	R_Y_LIST_05_MANUAL_L	0x30	RW	Bit[7:0]: Manual gamma curve Y list[5][7:0]
0x5DAA	R_Y_LIST_06_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[6][9:8]
0x5DAB	R_Y_LIST_06_MANUAL_L	0x38	RW	Bit[7:0]: Manual gamma curve Y list[6][7:0]
0x5DAC	R_Y_LIST_07_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[7][9:8]
0x5DAD	R_Y_LIST_07_MANUAL_L	0x40	RW	Bit[7:0]: Manual gamma curve Y list[7][7:0]
0x5DAE	R_Y_LIST_08_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[8][9:8]
0x5DAF	R_Y_LIST_08_MANUAL_L	0x48	RW	Bit[7:0]: Manual gamma curve Y list[8][7:0]
0x5DB0	R_Y_LIST_09_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[9][9:8]
0x5DB1	R_Y_LIST_09_MANUAL_L	0x50	RW	Bit[7:0]: Manual gamma curve Y list[9][7:0]

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address	register name	default value	R/W	description
0x5DB2	R_Y_LIST_10_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[10][9:8]
0x5DB3	R_Y_LIST_10_MANUAL_L	0x60	RW	Bit[7:0]: Manual gamma curve Y list[10][7:0]
0x5DB4	R_Y_LIST_11_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[11][9:8]
0x5DB5	R_Y_LIST_11_MANUAL_L	0x70	RW	Bit[7:0]: Manual gamma curve Y list[11][7:0]
0x5DB6	R_Y_LIST_12_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[12][9:8]
0x5DB7	R_Y_LIST_12_MANUAL_L	0x90	RW	Bit[7:0]: Manual gamma curve Y list[12][7:0]
0x5DB8	R_Y_LIST_13_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[13][9:8]
0x5DB9	R_Y_LIST_13_MANUAL_L	0xB0	RW	Bit[7:0]: Manual gamma curve Y list[13][7:0]
0x5DBA	R_Y_LIST_14_MANUAL_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Manual gamma curve Y list[14][9:8]
0x5DBB	R_Y_LIST_14_MANUAL_L	0xD0	RW	Bit[7:0]: Manual gamma curve Y list[14][7:0]
0x5DBC	R_MAX_SHADOW_H_GAIN	0xFF	RW	Bit[7:0]: Gamma maximum shadow h gain
0x5DBD	R_MID_TONE_H_GAIN	0x6E	RW	Bit[7:0]: Middle tone h gain
0x5DBE	R_HIGH_LIGHT_H_GAIN	0x10	RW	Bit[7:0]: High light h gain
0x5DBF	R_PARA_MANUAL_EN	0x00	RW	Manual Gamma Parameter Enable
0x5E00	RGB_DNS_CTRL0	0x0C	RW	Bit[7:6]: Not used Bit[5:1]: rgb_dns_shd_ext_noise Bit[0]: rgb_dns_smoothy_en
0x5E01	RGB_DNS_CTRL1	0x08	RW	Bit[7:4]: Not used Bit[3:0]: rgb_dns_edgethre
0x5E01	RGB_DNS_CTRL1	0x08	RW	Bit[7:4]: Not used Bit[3:0]: rgb_dns_edgethre
0x5E02	RGB_DNS_CTRL2	0x08	RW	Bit[7:6]: Not used Bit[5:3]: rgb_dns_ylist1 Bit[2:0]: rgb_dns_ylist0

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address	register name	default value	R/W	description
0x5E02	RGB_DNS_CTRL2	0x08	RW	Bit[7:6]: Not used Bit[5:3]: rgb_dns_ylist1 Bit[2:0]: rgb_dns_ylist0
0x5E03	RGB_DNS_CTRL3	0x1A	RW	Bit[7:6]: Not used Bit[5:3]: rgb_dns_ylist3 Bit[2:0]: rgb_dns_ylist2
0x5E04	RGB_DNS_CTRL4	0x24	RW	Bit[7:6]: Not used Bit[5:3]: rgb_dns_ylist5 Bit[2:0]: rgb_dns_ylist4
0x5E05	RGB_DNS_CTRL5	0x24	RW	Bit[7:6]: Not used Bit[5:3]: rgb_dns_ylist7 Bit[2:0]: rgb_dns_ylist6
0x5E06	RGB_DNS_CTRL6	0x02	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist0
0x5E07	RGB_DNS_CTRL7	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist1
0x5E08	RGB_DNS_CTRL8	0x06	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist2
0x5E09	RGB_DNS_CTRL9	0x08	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist3
0x5E0A	RGB_DNS_CTRLA	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist4
0x5E0B	RGB_DNS_CTRLB	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist5
0x5E0C	RGB_DNS_CTRLC	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist6
0x5E0D	RGB_DNS_CTRLD	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist7
0x5E0D	RGB_DNS_CTRLD	0x0A	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist7
0x5E0E	RGB_DNS_CTRLE	0x02	RW	Bit[7:4]: Not used Bit[3:1]: rgb_dns_ylist_man Bit[0]: rgb_dns_para_man_en
0x5E0F	RGB_DNS_CTRLF	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgb_dns_uvlist_man
0x5E10	RGB_DNS_CTRL10	–	R	Bit[7:3]: Not used Bit[2:0]: Final y_noise read out
0x5E11	RGB_DNS_CTRL11	–	R	Bit[7:6]: Not used Bit[5:0]: Final uv_noise read out

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address	register name	default value	R/W	description
0x5E80	R_NOISE_LIST_0	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[0]
0x5E81	R_NOISE_LIST_1	0x02	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[1]
0x5E82	R_NOISE_LIST_2	0x04	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[2]
0x5E83	R_NOISE_LIST_3	0x08	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[3]
0x5E84	R_NOISE_LIST_4	0x0C	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[4]
0x5E85	R_NOISE_LIST_5	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[5]
0x5E86	R_NOISE_LIST_6	0x14	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[6]
0x5E87	R_NOISE_LIST_7	0x18	RW	Bit[7:5]: Not used Bit[4:0]: Noise list[7]
0x5E88	R_CTRL	0x04	RW	Bit[7:6]: Reserved Bit[5]: Manual noise enable Bit[4:0]: Shadow extra noise
0x5E89	R_MANUAL_NOISE	0x0A	RW	Bit[7:5]: Not used Bit[4:0]: Manual noise
0x5E8A	RSVD	–	–	Reserved
0x5F00	R_CTRL00	0x00	RW	Bit[7:0]: Manual x start coordinate[15:8]
0x5F01	R_CTRL01	0x00	RW	Bit[7:0]: Manual x start coordinate[7:0]
0x5F02	R_CTRL02	0x00	RW	Bit[7:0]: Manual y start coordinate[15:8]
0x5F03	R_CTRL03	0x00	RW	Bit[7:0]: Manual y start coordinate[7:0]
0x5F04	R_CTRL04	0x02	RW	Bit[7:0]: Manual window width[15:8]
0x5F05	R_CTRL05	0xF0	RW	Bit[7:0]: Manual window width[7:0]
0x5F06	R_CTRL06	0x02	RW	Bit[7:0]: Manual window height[15:8]
0x5F07	R_CTRL07	0x08	RW	Bit[7:0]: Manual window height[7:0]
0x5F08	R_CTRL08	0x00	RW	Bit[7:3]: Not used Bit[2]: Flip offset enable Bit[1]: Mirror offset enable Bit[0]: Manual window setting enable
0x5F09~ 0x5F0C	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x6200	R_ADDR_BYTE	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Byte address space of SPI EEPROM 00: 1 byte 01: 2 bytes 10: 3 bytes 11: 4 bytes
0x6201	R_SCK_POL	0x00	RW	Bit[7:1]: Not used Bit[0]: ESCK polarity rev
0x6202	R_SPEED	0x04	RW	Bit[7:5]: Not used Bit[4:0]: EEPROM read speed 0x0: ESCK speed = pclk* 0x1: ESCK speed = pclk/2 0x2: ESCK speed = pclk/4 Others: PCLK freq = 2×sclk freq
0x6203	EOF_CLR	0x00	RW	Bit[7:1]: Not used Bit[0]: End of frame clear signal 0: Use SOF as overlay image load start for each frame 1: Use previous EOF as overlay image load start for each frame
0x6204	GRP_HLD	0x00	RW	Bit[7:1]: Not used Bit[0]: Group hold register 0: Index or resolution information load is allowed for each layer 1: Cannot load until grp_hold change to 0
0x6205	R_FRAME_COM	0x00	RW	Bit[7:1]: Not used Bit[0]: Frame compress mode 0: Compress one line mode frame compress. Need to read in overlay image information at beginning of a line. 1: Compress whole frame mode. Read in all overlay image information at beginning of a frame. There is no SPI interface in use during a frame.
0x6206	R_DLY	0x02	RW	Bit[7:5]: Not used Bit[4:0]: spi_ctrl request delay Adjust delay timing between two SPI control requests
0x6207~ 0x6208	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x6209	R_FAST_RD	0x01	RW	Bit[7:1]: Not used Bit[0]: Fast read command select signal, to make read command faster When enabled, corresponding fast read command should be 8'h0B (0x620F).
0x620A	R_ROUND_BACK	0x01	RW	Bit[7:1]: Not used Bit[0]: SPI read-in data and valid timing option
0x620B	R_GATE_EN	0x01	RW	Bit[7:1]: Not used Bit[0]: Internal SCK gate option
0x620D	R_OSD_CTRL	0x01	RW	Bit[7:2]: Not used Bit[1:0]: OSD control 0: Enable OSD function 1: Bypass OSD function
0x620E	RSVD	–	–	Reserved
0x620F	R_FAST_RD_CMD	0x0B	RW	Bit[7:0]: Fast read instruction Default is 8'h0B, synchronize with 0x6209
0x6210	R_RD_CMD	0x03	RW	Bit[7:0]: Normal read instruction Synchronize with 0x6209
0x6211	R_INDEX0_T_L	0x01	RW	Bit[7:0]: Overlay image 0 index[7:0]
0x6212	R_INDEX1_T_L	0x02	RW	Bit[7:0]: Overlay image 1 index[7:0]
0x6213~ 0x6214	RSVD	–	–	Reserved
0x6215	R_INDEX0_T_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Overlay image 0 index[9:8]
0x6216	R_INDEX1_T_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Overlay image 1 index[9:8]
0x6217~ 0x6218	RSVD	–	–	Reserved
0x6219	R_OV_RESO0_T	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Image resolution for layer1 0: Overlay image disabled 1: Overlay image resolution 1x1
0x621A	R_OV_RESO1_T	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Resolution for layer1
0x621B~ 0x621C	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x621D	R_X_START0_T_L	0x00	RW	Bit[7:0]: X start address for layer 0[7:0]
0x621E	R_Y_START0_T_L	0x00	RW	Bit[7:0]: Y start address for layer 0[7:0]
0x621F	R_X_START0_T_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X start address for layer 0[11:8]
0x6220	R_Y_START0_T_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y start address for layer 0[11:8]
0x6221	R_X_START1_T_L	0x00	RW	Bit[7:0]: X start address for layer 1[7:0]
0x6222	R_Y_START1_T_L	0x00	RW	Bit[7:0]: Y start address for layer 1[7:0]
0x6223	R_X_START1_T_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: X start address for layer 1[11:8]
0x6224	R_Y_START1_T_H	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Y start address for layer 1[11:8]
0x6225~ 0x622C	RSVD	–	–	Reserved
0x622D	SCCB_WDATA	0x00	RW	Bit[7:0]: SCCB write data
0x622E	LAY0_SEL	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Layer0 select 00: Select image0 stored in EEPROM as layer0 image 01: Select image1 stored in EEPROM as layer0 image 10: Select image2 stored in EEPROM as layer0 image (This number has to be a valid image number in EEPROM or load image will fail)
0x622F	LAY1_SEL	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Layer1 select 00: Select image0 stored in EEPROM as layer1 image 01: Select image1 stored in EEPROM as layer1 image 10: Select image2 stored in EEPROM as layer1 image (This number has to be a valid image number in EEPROM or load image will fail)
0x6230~ 0x6231	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x6232	R_LD_INDEX	0x00	RW	Bit[7:0]: Loading index 00: Select setting 0 stored in EEPROM to load 01: Select setting 1 stored in EEPROM to load 10: Select setting 2 stored in EEPROM to load (this number has to be a valid setting file number in EEPROM or load setting function will fail)
0x6233	R_AUTOMOVY_EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: Y auto move function enable for layer0
0x6234	R_AUTOMOVY_EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: Y auto move function enable for layer1
0x6235~ 0x6236	RSVD	–	–	Reserved
0x6237	R_AUTOMOVX_EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: X auto move function enable for layer0
0x6238	R_AUTOMOVX_EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: X auto move function enable for layer1
0x6239~ 0x623A	RSVD	–	–	Reserved
0x623B	R_AUTOMOVY_WRAP_ EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto move function Y wrap enable for layer0
0x623C	R_AUTOMOVY_WRAP_ EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto move function Y wrap enable for layer1
0x623D~ 0x623E	RSVD	–	–	Reserved
0x623F	R_AUTOMOVX_WRAP_ EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto move function X wrap enable for layer0
0x6240	R_AUTOMOVX_WRAP_ EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto move function X wrap enable for layer1
0x6241~ 0x6242	RSVD	–	–	Reserved

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address	register name	default value	R/W	description
0x6243	R_AUTOMV_STEP_SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto move step select 0: Step enabled 1: Step only, enabled at frames with auto change step pre-defined
0x6244	RSVD	–	–	Reserved
0x6245	R_SPI_SELN	0x00	RW	Bit[7:1]: Not used Bit[0]: SPI load select
0x6246	R_LD_PAD_DIS	0x00	RW	Bit[7:1]: Not used Bit[0]: Load pad disable
0x6247	R_LD_TRIGGER	0x01	RW	Bit[7:2]: Not used Bit[1:0]: Load trigger control 0: Power on load disable 1: Manual load setting function trigger
0x6248	RSVD	–	–	Reserved
0x6249	R_RETRY	0x02	RW	Bit[7:2]: Not used Bit[1:0]: Loading settings retry times
0x624A	R_SEQ_NU	0xFF	RW	Bit[7:0]: OSD_SEQ sequencer byte number
0x624B	R_TOGCNT_OR_RBLANKLINENU	0x20	RW	Bit[7:0]: Toggle counter or blanking lines number
0x624C	R_READ_ONCE0	0x00	RW	Bit[7:1]: Not used Bit[0]: FIFO write enable and FIFO read enable select signal for layer0
0x624D	R_READ_ONCE1	0x00	RW	Bit[7:1]: Not used Bit[0]: FIFO write enable and FIFO read enable select signal for layer1
0x624E~ 0x624F	RSVD	–	–	Reserved
0x6250	R_RETRY_PON	0x01	RW	Bit[7:1]: Not used Bit[0]: Retry only when power on
0x6251	RSVD	–	–	Reserved
0x6252	R_LD_BLANK	0x01	RW	Bit[7:1]: Not used Bit[0]: Loading blank 0: Do not load setting until blanking 1: Load setting at any time

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address	register name	default value	R/W	description
0x6253	R_AUTOCHG_WRAP_EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto change wrap enable for layer0
0x6254	R_AUTOCHG_WRAP_EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto change wrap enable for layer1
0x6255~0x6256	RSVD	–	–	Reserved
0x6257	R_AUTOCHG_EN0	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto change enable for layer0
0x6258	R_AUTOCHG_EN1	0x00	RW	Bit[7:1]: Not used Bit[0]: Auto change enable for layer1
0x6259~0x625A	RSVD	–	–	Reserved
0x625B	R_AUTOCHG_STIDX0_L	0x00	RW	Bit[7:0]: Auto change start index for layer0[7:0]
0x625C	R_AUTOCHG_EDIDX0_L	0x00	RW	Bit[7:0]: Auto change end index for layer0[7:0]
0x625D	R_AUTOCHG_STIDX1_L	0x00	RW	Bit[7:0]: Auto change start index for layer1[7:0]
0x625E	R_AUTOCHG_EDIDX1_L	0x00	RW	Bit[7:0]: Auto change end index for layer1[7:0]
0x625F~0x6262	RSVD	–	–	Reserved
0x6263	R_AUTOCHG_STIDX0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Auto change start index for layer0[9:8]
0x6264	R_AUTOCHG_EDIDX0_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Auto change end index for layer0[9:8]
0x6265	R_AUTOCHG_STIDX1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Auto change start index for layer1[9:8]
0x6266	R_AUTOCHG_EDIDX1_H	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Auto change end index for layer1[9:8]
0x6267~0x626A	RSVD	–	–	Reserved
0x626B	R_AUTOCHG_STEP_L	0x00	RW	Bit[7:0]: Auto change step[7:0]
0x626C	R_AUTOCHG_STEP_H	0x00	RW	Bit[7:0]: Auto change step[15:8]

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address	register name	default value	R/W	description
0x626D	R_AUTOMOVY_STEP0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Auto move Y step for layer0
0x626E	R_AUTOMOVX_STEP0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Auto move X step for layer0
0x626F	R_AUTOMOVY_STEP1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Auto move Y step for layer1
0x6270	R_AUTOMOVX_STEP1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Auto move X step for layer1
0x6271~ 0x6274	RSVD	–	–	Reserved
0x6275	OSD_ERR_ST_H	–	R	Bit[7:0]: OSD error state[15:8]
0x6276	OSD_ERR_ST_L	–	R	Bit[7:0]: OSD error state[7:0]
0x627F	R_YUV_Y_VAL	0x03	RW	Bit[7:2]: Not used Bit[1:0]: Overlay image y low 2 bits added value
0x6280	R_LD_WB_ADRHI_H	0x00	RW	Bit[7:0]: Wishbone address bus[15:8] for load setting function
0x6281	R_LD_WB_ADRHI_L	0x06	RW	Bit[7:0]: Wishbone address bus[7:0] for load setting function
0x6282	R_LD_DONE_O	–	R	Bit[7:1]: Not used Bit[0]: Flag to indicate load setting process is done
0x6283	R_OVEN_PAD_O	–	R	Bit[7:1]: Not used Bit[0]: Read only signal of oven pad value
0x6700~ 0x6718	RSVD	–	–	Reserved
0x6719	TPM_O1_L	–	R	TPM_O1_L
0x671A~ 0x6721	RSVD	–	–	Reserved
0xC2F0	S_MANUAL_EXP11	0x34	RW	Bit[7:0]: Frame_A_manual_long_exp[15:8] Frame A manual long channel exposure
0xC2F1	S_MANUAL_EXP11	0x00	RW	Bit[7:0]: Frame_A_manual_long_exp[7:0] Frame A manual long channel exposure
0xC2F2	S_MANUAL_EXP12	0x06	RW	Bit[7:0]: Frame_A_manual_short_exp[15:8] Frame A manual short channel exposure

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table A-1 sensor control registers (sheet 110 of 112)

address	register name	default value	R/W	description
0xC2F3	S_MANUAL_EXP12	0x80	RW	Bit[7:0]: Frame_A_manual_short_exp[7:0] Frame A manual short channel exposure
0xC2F4	S_MANUAL_EXP21	0x34	RW	Bit[7:0]: Frame_B_manual_long_exp[15:8] Frame B manual long channel exposure
0xC2F5	S_MANUAL_EXP21	0x00	RW	Bit[7:0]: Frame_B_manual_long_exp[7:0] Frame B manual long channel exposure
0xC2F6	S_MANUAL_EXP22	0x06	RW	Bit[7:0]: Frame_B_manual_short_exp[15:8] Frame B manual short channel exposure
0xC2F7	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: Frame_B_manual_short_exp[7:0] Frame B manual short channel exposure
0xC2F8	S_MANUAL_EXP31	0x34	RW	Bit[7:0]: Frame_C_manual_long_exp[15:8] Frame C manual long channel exposure
0xC2F9	S_MANUAL_EXP31	0x00	RW	Bit[7:0]: Frame_C_manual_long_exp[7:0] Frame C manual long channel exposure
0xC2FA	S_MANUAL_EXP32	0x06	RW	Bit[7:0]: Frame_C_manual_short_exp[15:8] Frame C manual short channel exposure
0xC2FB	S_MANUAL_EXP22	0x80	RW	Bit[7:0]: Frame_C_manual_short_exp[7:0] Frame C manual short channel exposure
0xC2FC	S_MANUAL_GAIN11	0x10	RW	Bit[7:0]: Frame_A_manual_long_gain[15:8] Frame A manual long channel gain
0xC2FD	S_MANUAL_GAIN11	0x18	RW	Bit[7:0]: Frame_A_manual_long_gain[7:0] Frame A manual long channel gain
0xC2FE	S_MANUAL_GAIN12	0x10	RW	Bit[7:0]: Frame_A_manual_short_gain[15:8] Frame A manual short channel gain
0xC2FF	S_MANUAL_GAIN12	0x18	RW	Bit[7:0]: Frame_A_manual_short_gain[7:0] Frame A manual short channel gain
0xC300	S_MANUAL_GAIN21	0x10	RW	Bit[7:0]: Frame_B_manual_long_gain[15:8] Frame B manual long channel gain
0xC301	S_MANUAL_GAIN21	0x18	RW	Bit[7:0]: Frame_B_manual_long_gain[7:0] Frame B manual long channel gain

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table A-1 sensor control registers (sheet 111 of 112)

address	register name	default value	R/W	description
0xC302	S_MANUAL_GAIN22	0x10	RW	Bit[7:0]: Frame_B_manual_short_gain[15:8] Frame B manual short channel gain
0xC303	S_MANUAL_GAIN22	0x18	RW	Bit[7:0]: Frame_B_manual_short_gain[7:0] Frame B manual short channel gain
0xC304	S_MANUAL_GAIN31	0x10	RW	Bit[7:0]: Frame_C_manual_long_gain[15:8] Frame C manual long channel gain
0xC305	S_MANUAL_GAIN31	0x18	RW	Bit[7:0]: Frame_C_manual_long_gain[7:0] Frame C manual long channel gain
0xC306	S_MANUAL_GAIN32	0x10	RW	Bit[7:0]: Frame_C_manual_short_gain[15:8] Frame C manual short channel gain
0xC307	S_MANUAL_GAIN32	0x18	RW	Bit[7:0]: Frame_C_manual_short_gain[7:0] Frame C manual short channel gain
0xC308	S_MANUAL_EN	0x00	RW	Bit[0]: AB or ABC manual exposure/gain mode enable 0: Disable 1: Enable
0xC309	S_MANUAL_MODE	0x00	RW	Bit[2]: Frame A manual exposure/gain enable 0: Disable 1: Enable Bit[1]: Frame B manual exposure/gain enable 0: Disable 1: Enable Bit[0]: Frame C manual exposure/gain enable 0: Disable 1: Enable
0xC30A	S_MANUAL_DONE	0x00	RW	Bit[1:0]: A, B and C frame manual exposure/gain enable 00: Sensor does not take new manual exposure/gain 01: Sensor takes manual exposure/gain once upon register 0xC30A setting to 1 10: Sensor always takes manual exposure/gain as long as register 0xC30A is 2
0xC34A	MAX STAGE3 OFFSET MSB	0x02	RW	Bit[7:0]: Max_stage3_offset[15:8] Maximum offset subtracted from pixel output in third BLC stage

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table A-1 sensor control registers (sheet 112 of 112)

address	register name	default value	R/W	description
0xC34B	MAX STAGE3 OFFSET LSB	0x00	RW	Bit[7:0]: Max_stage3_offset[7:0] Maximum offset subtracted from pixel output in third BLC stage

revision history

version 1.0 10.14.2015

- initial release

version 1.01 10.30.2015

- in key specifications, added stable image temperature range
- in table 9-2, added stable image temperature range

version 1.02 02.04.2016

- in ordering information, changed ordering part number to "OV07850-N02A-PE (color, lead-free) 102-pin mCSP™, rev 1E, packed in tray with protective film" and added ordering part number "OV07850-N02A (color, lead-free) 102-pin mCSP™, rev 1E, packed in tray"

version 1.1 02.12.2016

- in table 9-3, added max values for I_{DD-A}, I_{DD-D}, I_{DD-IO}, $I_{DDS-PWDN-A}$, $I_{DDS-PWDN-D}$, and $I_{DDS-PWDN-IO}$
- in table 9-3, changed typ value for $I_{DDS-PWDN-A}$ to 10 µA

version 1.11 03.11.2016

- in table 3-2, changed default value for register 0x3809 to 0x88 and changed default value for register 0x380B to 0xE8
- in table A-1, changed default value for register 0x3809 to 0x88 and changed default value for register 0x380B to 0xE8

version 1.12 03.24.2016

- in features, removed last two bullets

version 1.13 06.04.2016

- in table 1-1, removed "/strobe" from FSIN signal description
- in table 3-5, changed register description for 0x3025[5] binary value selection 0 to "Not used"
- in table A-1, changed register description for 0x3025[5] binary value selection 0 to "Not used"

version 1.14 01.30.2017

- in chapter 9, added section 9.5, including tables 9-6 and 9-7

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version 2.0 04.18.2017

- changed datasheet from Preliminary Specification to Product Specification
- in table 9-3, changed max value for input capacitor (C_{IN}) to 10pF

version 2.01 09.12.2017

- in key specifications, removed bullet for dark current

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